Department of Electrical Engineering
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ELEG3923 Microprocessor
Ch.8 Hardware Connection

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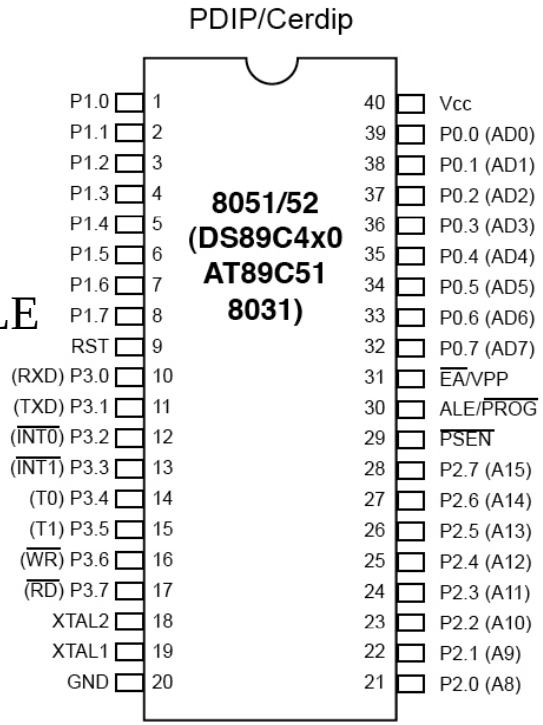
OUTLINE

- **Pin description**
- **DS89C4x0 Trainner**
- **Intel Hex file**

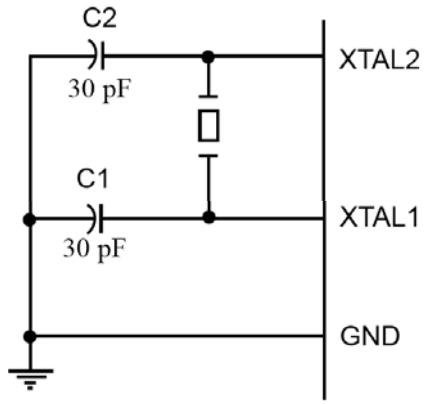
PIN: LAYOUT

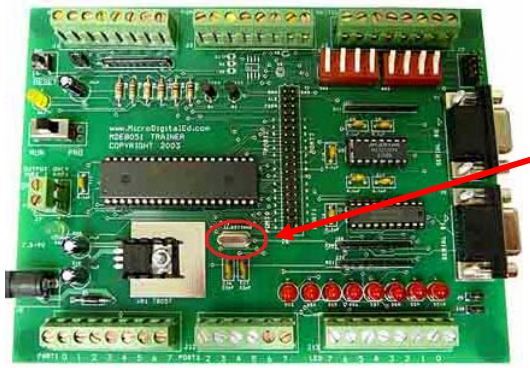
- **Pin layout**
  - A total of 40 pins
  - 32 pins are used for I/O ports (8 pins/port, 4 ports)
  - The remaining 8 pins
    - Vcc, GND, XTAL1, XTAL2, RST, $\overline{EA}$, $\overline{PSEN}$, ALE
- **Vcc**
  - Pin 40. Provide supply voltage to the chip.
  - Voltage source is +5V.
- **GND**
  - Pin 20. Ground

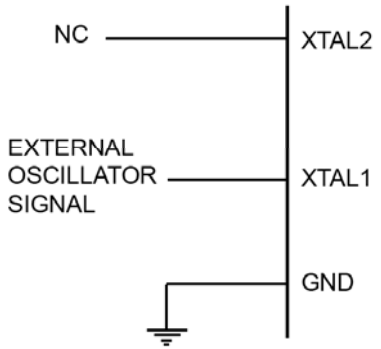


PIN: XTAL1 AND XTAL2

- **XTAL1 and XTAL2**
  - Provide external clock to the 8051 (input pins)
  - Configuration 1 (most common):
    - Connect to a quartz crystal oscillator
    - Crystal oscillator can generate square waveform at a fixed frequency (e.g. 11.0592 MHz)
    - Different 8051 chips have different speed ratings
      - E.g. a 12-MHz chip can only be connected to a crystal oscillator with frequency 12 MHz or lower.
    - We can observe the clock with an oscilloscope on XTAL2 pin
  - Configuration 2:
    - Connect it to an external TTL oscillator (e.g. a clock signal generated by a function generator)
    - Only XTAL1 is used, XTAL2 is left unconnected (NC: not connected)





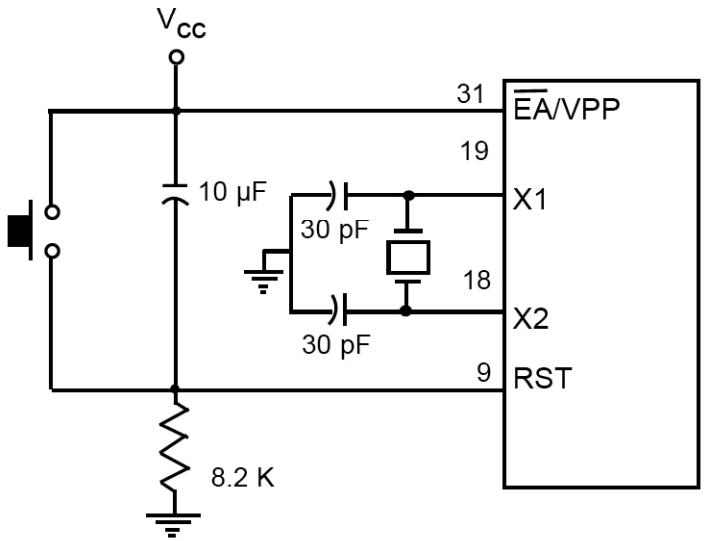


PIN: RST

- **RST**
  - Reset (input pin)
  - Active high: upon applying a high pulse to the pin, the uC will reset and terminate all activities.
    - Normally it's value is low so uC can work normally.
    - In order for it too be effective, the high pulse must be high for a minimum of 2 machine cycles.
  - Reset by switch
    - When SW is open, RST is low
    - When SW is closed, RST is high

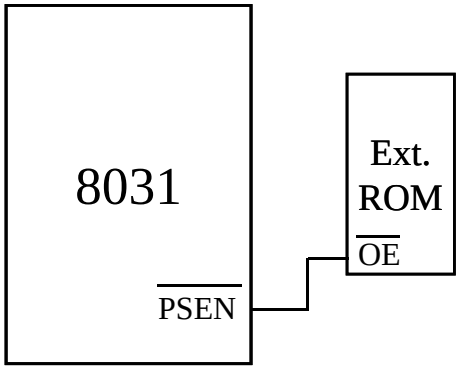
      When SW is released, RST is low

      → reset.
  - Power on reset
    - At the instant of power on, RST is high
    - After a while, the capacitor will be fully charged
    - In steady state, RST is low.



PIN: $\overline{EA}$, $\overline{PSN}$, AND ALE

- **8031**
  - A simplified version of 8051, it doesn't have built in ROM or RAM
  - It needs to be connected to external ROM and RAM through ~~EA~~, ~~PSN~~, and ALE
- **$\overline{EA}$**
  - External access (input pin): indicate whether there is external ROM
  - Active low: it's effective when the voltage is low
  - If it is connected to ground → there is external ROM
  - If it is connected to Vcc → there is no external ROM
- **$\overline{PSEN}$**
  - Program store enable. (output pin)
  - If external ROM is connected to the uC, this pin is connected to the OE (output enable) pin of the ROM to enable the output of the ROM.
  - Active low: it's effective when the voltage is low



- **ALE**
  - Address latch enable (output pin)
  - Port 0 is used as both address bus and data bus for external RAM
  - If it's high, then P0 is used as address bus; if it's low, then P0 is used as data bus.

PIN: DEFAULT VALUES

- **The default value of some 8051 registers upon reset**

Register	Reset Value (hex)
PC	0000
DPTR	0000
ACC	00
PSW	00
SP	07
B	00
P0-P3	FF

- **Machine cycle and crystal frequency**

Chip (Maker)	Clocks per Machine Cycle
AT89C51/52 (Atmel)	12
P89C54X2 (Phillips)	6
DS5000 (Dallas Semiconductor)	4
DS89C4x0 (Dallas Semiconductor)	1

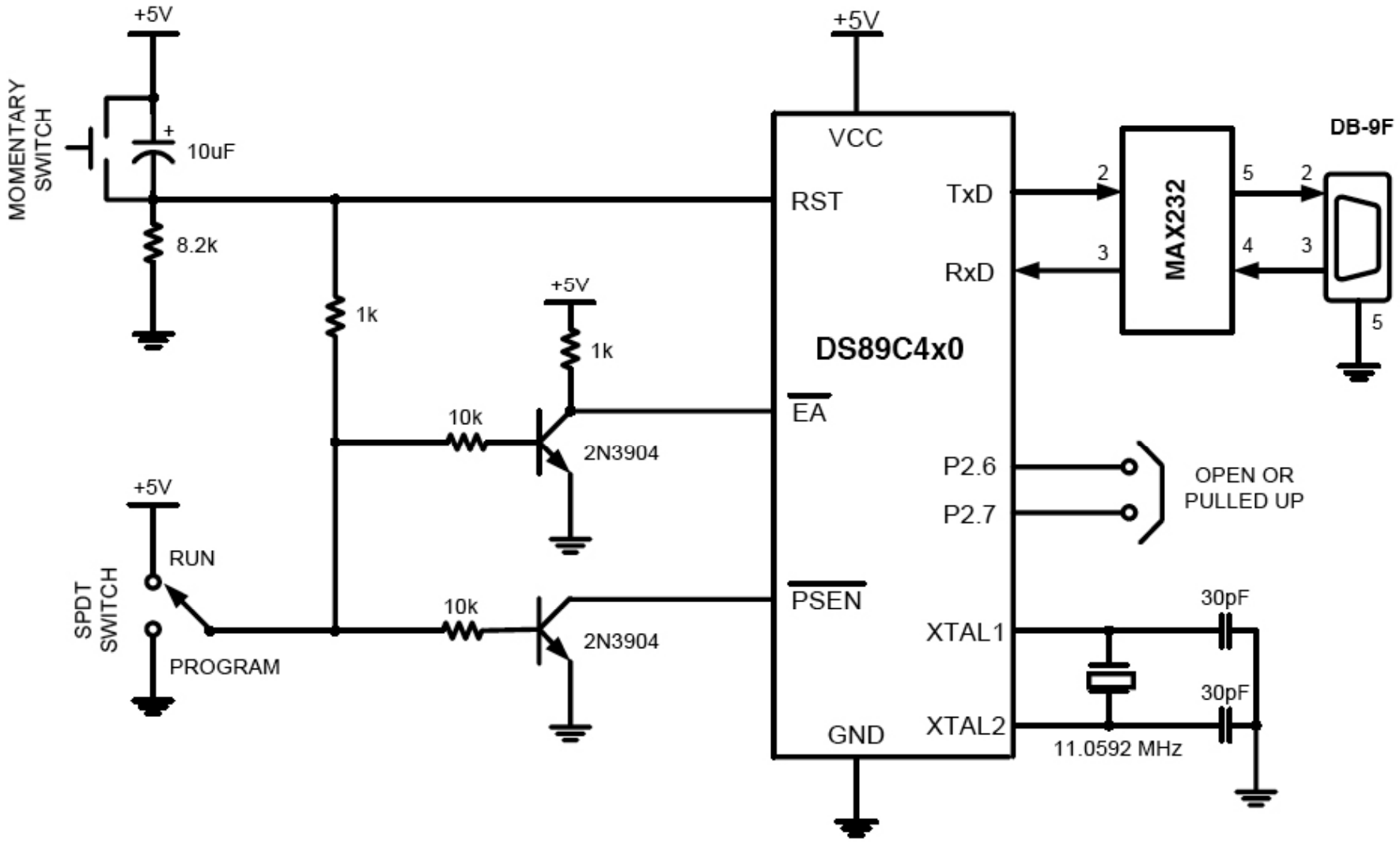
OUTLINE

- Pin description
- **DS89C4x0 HardwareTrainer**
- Intel Hex file

HARDWARE: KEY FEATURES

- **Key features of DS89C4x0**
  - On chip flash ROM
    - DS89C420/30: 16KB
    - DS89C440: 32KB
    - DS89C450: 64KB
  - High speed
    - 1 clock per machine cycle
    - DC to 33 MHz operation (it can be connected to a crystal with freq. 33KMHz)
  - 256 bytes RAM
  - Two full duplex serial ports
  - 13 interrupt sources (6 external) with 5 level of interrupt priority
  - Programmable watchdog timer.

HARDWARE


+5V
MOMENTARY SWITCH
10uF
8.2k
1k
+5V
1k
10k
2N3904
+5V
RUN
SPDT SWITCH
PROGRAM
10k
2N3904
+5V
VCC
RST
DS89C4x0
EA
PSEN
GND
TxD
RxD
P2.6
P2.7
XTAL1
XTAL2
2
3
MAX232
5
4
2
3
DB-9F
5
OPEN OR PULLED UP
30pF
30pF
11.0592 MHz

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- **Pin description**
- **DS89C4x0 HardwareTrainer**
- **Intel Hex file**

INTEL HEX FILE

- **Intel hex file**
  - A widely used file format designed to standardize the loading of executable machine code into a ROM chip
  - Review:
    - Source code → Obj file (optional: list file) → Absolute file → Hex file

assembler — linker — Object-to-hex converter

- **Format of hex file**

```
:10000000758055759055 75A0557DFA111C7580AA9F
:100010007590AA75A0AA7DFA111C80E47C237B4F01
:07002000DBFEDCFADDF62235
:00000001FF
```

  - It can be open by using any text editor
  - Each line can be decomposed into 4 fileds

```
:CC   AAAA TT   DDDDDDDDDDDDDDDDDDDDDDDDDDDDDDDD   SS
:10   0000 00   7580557590557 5A0557DFA111C7580AA   9F
:10   0010 00   7590AA75A0AA7DFA111C80E47C237B4F   01
:07   0020 00   DBFEDCFADDF622                      35
:00   0000 01   FF
```

INTEL HEX FILE

- **Format of Intel hex file**
  - Each line starts with a colon
  - CC: the number of bytes in this line, the maximum value of 10H
  - AAAA: a 16-bit address indicating where the contents of the line should be stored in ROM
  - TT: type. If TT=00, then this is not the last line; if TT=01, this is the last line.
  - DD…DDD: the real data or code to be stored in ROM
  - SS: checksum for everything in the line to make sure there is no error.
  - It always ends with FF.

```
:CC   AAAA TT   DDDDDDDDDDDDDDDDDDDDDDDDDDDDDDDD   SS
:10   0000 00   7580557590557 5A0557DFA111C7580AA   9F
:10   0010 00   7590AA75A0AA7DFA111C80E47C237B4F   01
:07   0020 00   DBFEDCFADDF622                      35
:00   0000 01   FF
```

INTEL HEX FILE

List file

```
LOC  OBJ       LINE
0000           1              ORG 0H
0000 758055    2    MAIN:     MOV P0, #55H
0003 759055    3              MOV P1, #55H
0006 75A055    4              MOV P2, #55H
0009 7DFA      5              MOV R5, #250
000B 111C      6              ACALL MSDELAY
000D 7580AA    7              MOV P0, #0AAH
0010 7590AA    8              MOV P1, #0AAH
0013 75A0AA    9              MOV P2, #0AAH
0016 7DFA      10             MOV R5, #250
0018 111C      11             ACALL MSDELAY
001A 80E4      12             SJMP MAIN
               13 ;--- THE 250 MILLISECOND DELAY.
               14   MSDELAY:
001C 7C23      15   HERE3:    MOV R4, #35
001E 7B4F      16   HERE2:    MOV R3,#79
0020 DBFE      17   HERE1:    DJNZ R3, HERE1
0022 DCFA      18             DJNZ R4, HERE2
0024 DDF6      19             DJNZ R5, HERE3
0026 22        20             RET
               21             END
```

Hex file

```
:CC  AAAA TT  DDDDDDDDDDDDDDDDDDDDDDDDDDDDDDDD  SS
:10  0000 00  75805575905575A0557DFA111C7580AA   9F
:10  0010 00  7590AA75A0AA7DFA111C80E47C237B4F   01
:07  0020 00  DBFEDCFADDF622                     35
:00  0000 01  FF
```