8051 - Interfacing

EE4380 Fall 02

Class 5

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8051 Interfacing

- 8051 Pinout
- Functions of the 8051 pins
- Power-On Reset
- Clock
- Address and data Bus
- External Vs On-chip code memory
- 8051 Interfacing basics
- Address Map and Address Generation

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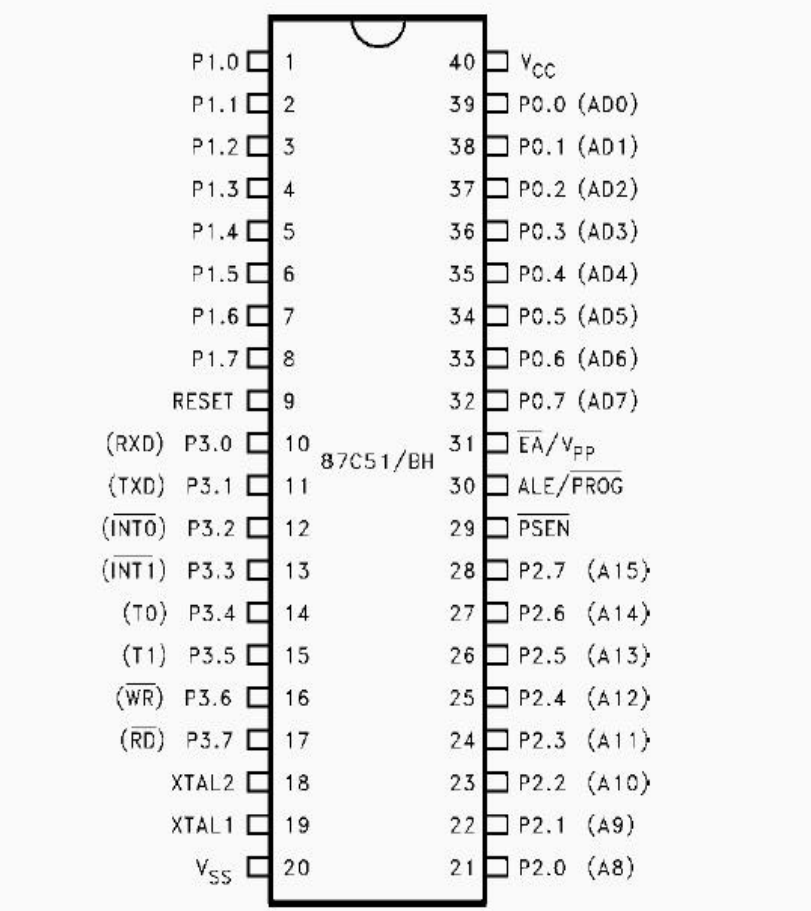
8051 Pinout

- Power - Vcc, Vss
- Reset - RST
- Crystal - XTAL[1,2]
- External device interfacing
  - EA, ALE, PSEN, WR, RD
- I/O Port
  - P0[7;0], P1[7:0], P2[7:0], P3
- P3 is shared with control lines
  - Serial I/O RxD, TxD,
  - external interrupts INT0, INT1
  - Counter control T0, T1
- P0 and P2 are multiplexed with Address and Data bus



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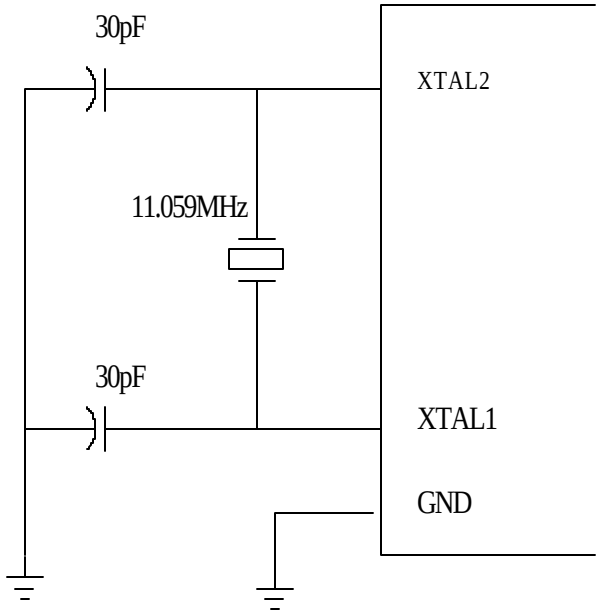
8051 Clock

- 8051 has an on-chip oscillator
- It needs an external crystal
- Standard connection as shown
- Crystal decides the operating frequency of the 8051



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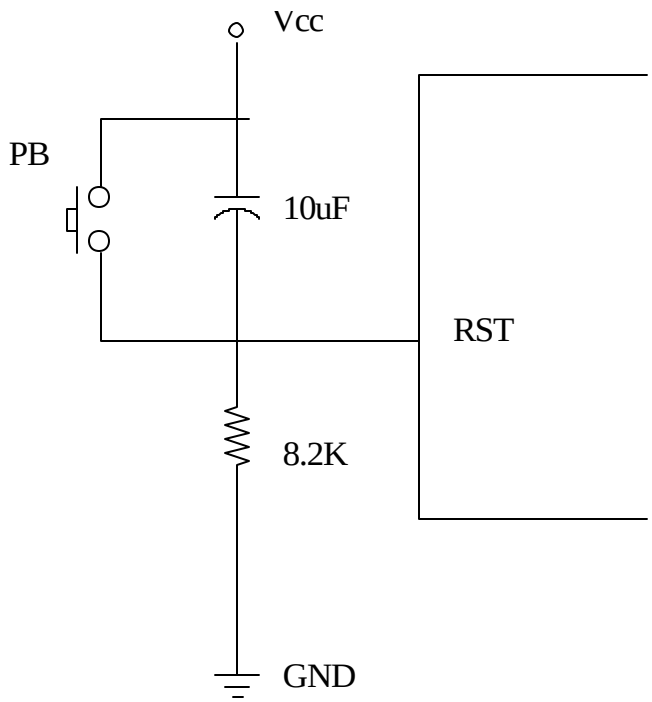
8051 Reset

- RESET is an active High input
- When RESET is set to High, 8051 goes back to the power-on state
- Power-On Reset
  - Push PB and active High on RST
  - Release PB, Capacitor discharges and RST goes low
- RST must stay high for a min of 2 machine cycles



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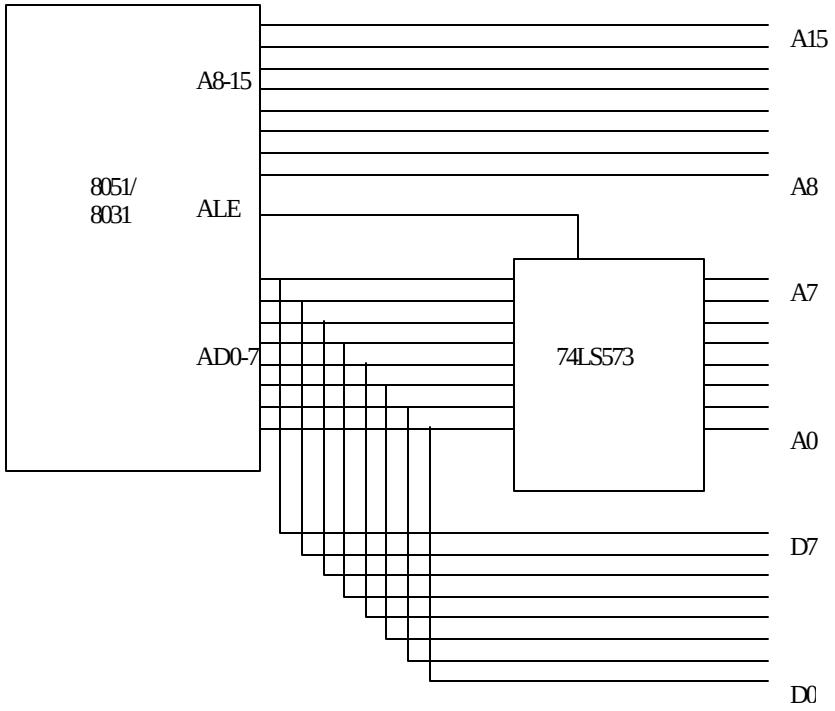
8051 – Address Bus Demuxing

- ALE – Address Latch Enable
- 8051 drives it high when address is available on AD[7,0]
- ALE is used as the “Enable” signal for an external latch (74LS573 or 373)
- P0 and P2 unavailable



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8051 External Code mem Access

- 8051 devices can have either on-chip or external code ROM
- Special pin EA decides which is used and PSEN is used to enable it.
- EA is an active low input to 8051
  - EA connected to GND (Low) means 8051 uses external memory for code
  - EA connected to Vcc (High) means 8051 uses on-chip ROM for code memory
- PSEN – Program Store Enable, active low
  - Connect this to the OE (output enable) of external ROM device

Microprocessor Interfacing - Basics

- Any CPU (8051) has
  - Address bus A[15:0]
  - Data bus D[7:0]
  - Control lines : PSEN, RD, WR
- A Single Processor uP based system has one CPU and many devices **interfaced** to it
- Only one Address bus and one data bus in a Single Processor system
  - ABUS and DBUS are common for all interfaced devices and the CPU

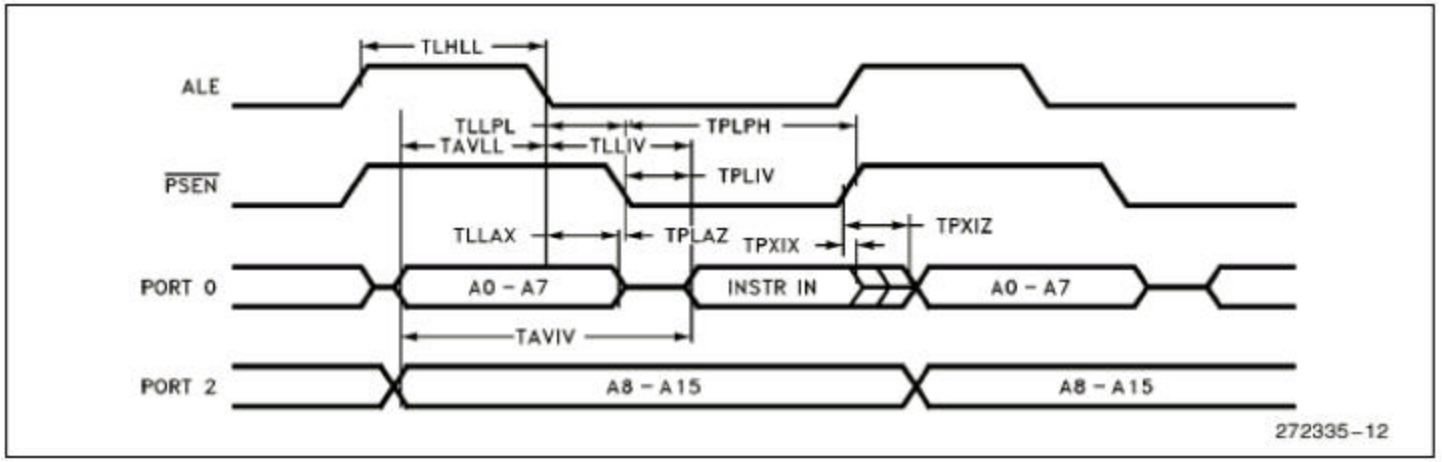
Microprocessor Interfacing (contd.)

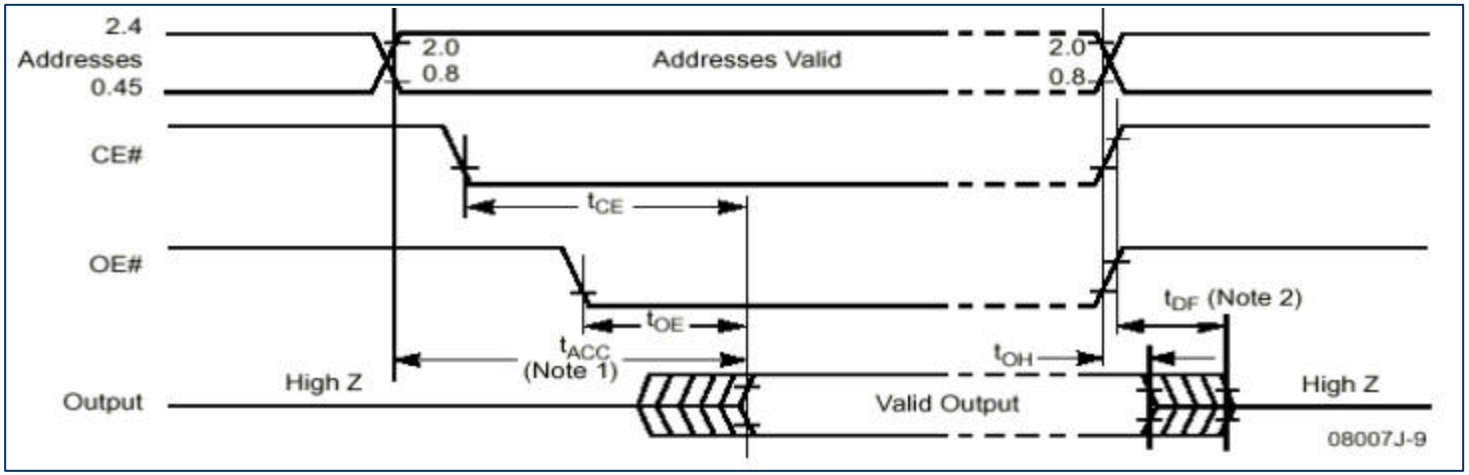
- All Microprocessor compatible devices have enable lines (CE - Chip Enable or CS - Chip Select)
  - A **function** of the address bus ***f(A[15:0])*** is connected to the CE of every device interfaced
  - This function is **unique** for every interfaced device
- The CPU accesses each interfaced device by way of this unique function
  - This function is commonly referred to as the ***address of the device***

Microprocessor Interfacing (contd.)

- Interfaced devices either READ or WRITE or do BOTH on the DBUS.
  - Only one device has "***exclusive access***"
  - Achieved by using Tri-State buses
- Devices that WRITE to DBUS have CE and RD/OE only
  - Read Cycle: Assert CE and then assert RD/OE
- Devices that READ and WRITE to DBUS have CE, RD/OE and WR
  - Write Cycle: Assert CE and then assert WR

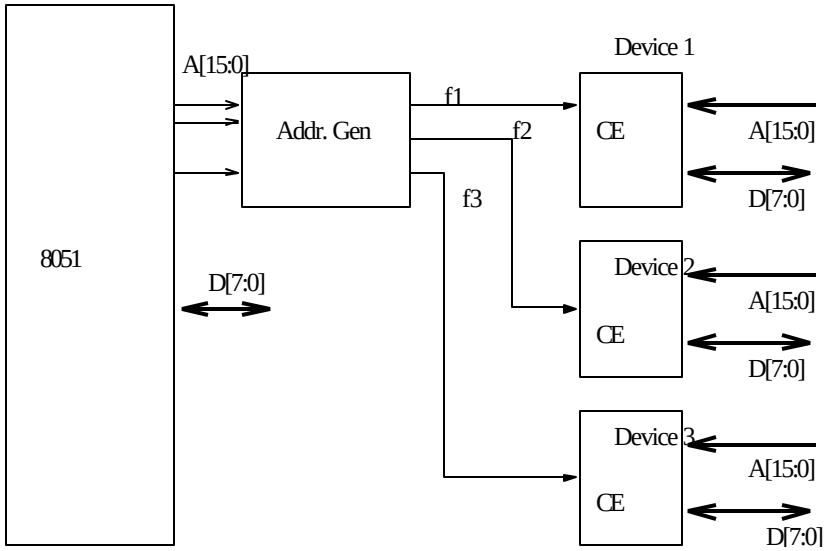
8051 Ext. Code Mem Read Cycle





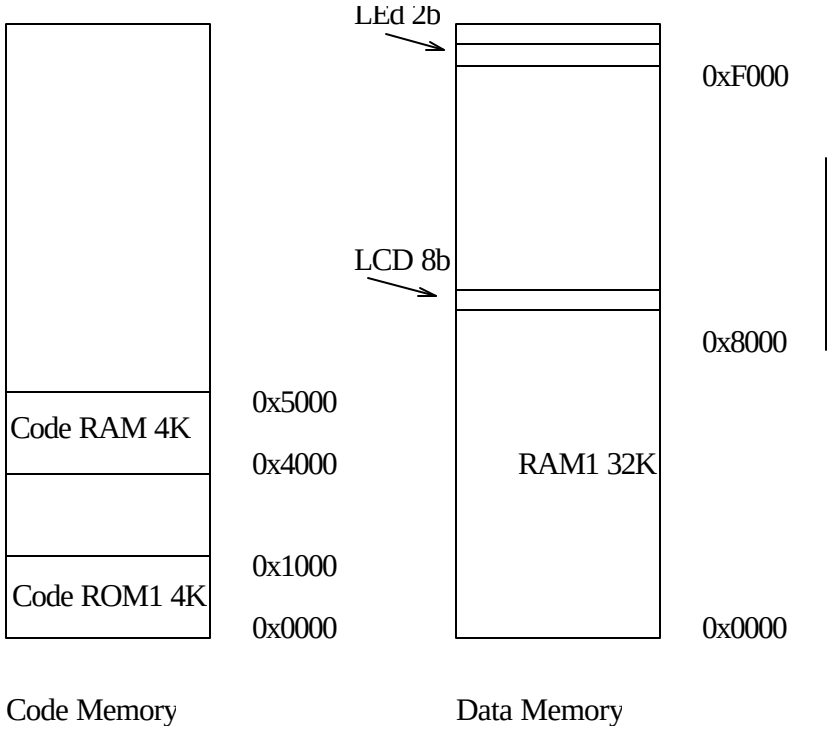
8051 – Address Generation

- Address Generator is a piece of hardware that produces unique addresses to each interfaced device
- Example
  - F1 = A15 . A14
  - F2 = A15 . A14’
  - F3 = A15’. A14’



8051- Address Map

- Address Map
  - List of addresses of all interfaced devices
  - List of sizes of each interfaced device
- Example
  - 4K of Code Rom at 0x0000
  - 4K of Code RAM at 0x4000
  - 32K of Data RAM at 0x0000
  - 16 bytes of Data RAM (LCD) at 0x 8000
  - 2bytes of Data RAM (7 seg LEDs) at 0xF000



Thanks

- Next Class
  - How to design the address generator ?
  - Interface external memory – Data, Code, data+Code
  - Interface external non-memory devices – ADC, LCD
  - Timing considerations for interfacing