Advanced Microprocessors

An Overview of ARM Cores
and Processors IP

ARM Processor Cores Overview

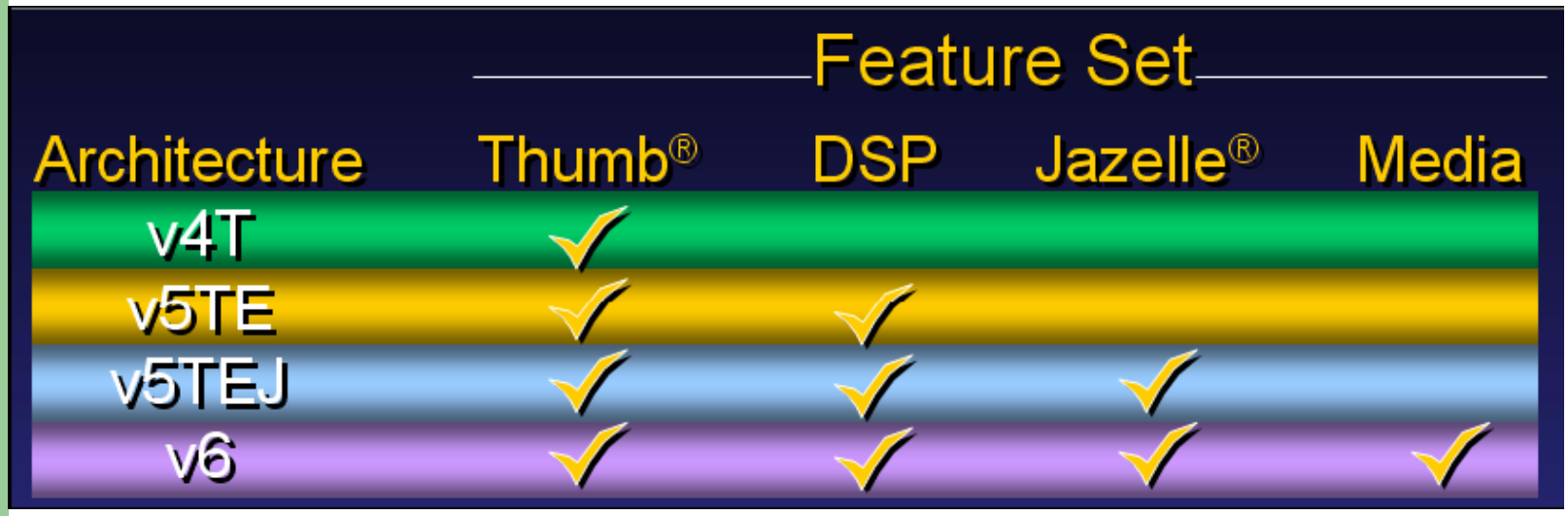
- ARM is the industry's leading provider of 32-bit embedded RISC microprocessors with almost 75% of the market*.
- ARM offers a wide range of processor cores based on a common architecture and delivering high performance together with low power consumption and system cost.
- The ARM processor range provides solutions for:
  - **Open platforms** running complex operating systems for wireless, consumer and imaging applications.
  - **Embedded real-time systems** for mass storage, automotive, industrial and networking applications.
  - **Secure applications** including smart cards and SIMs.

ARM Architecture Capabilities

- The ARM architecture provides support for the 32-bit ARM and 16-bit Thumb® Instruction Set Architectures (ISAs) along with architecture extensions to provide support for Java acceleration (Jazelle™) and security (TrustZone™) technologies.
- The ARM ISA is constantly improving to meet the increasing demands of leading edge applications developers, while retaining the backwards compatibility necessary to protect investment in software development.

Architecture	Thumb®	DSP	Jazelle	Media	TrustZone	Thumb-2
v4T	✔					
v5TE	✔	✔				
v5TEJ	✔	✔	✔			
v6	✔	✔	✔	✔		
v6Z	✔	✔	✔	✔	✔	
v6T2	✔	✔	✔	✔		✔

Performance Architectures



- Enhance performance through innovation
  - Thumb® up to 35% code compression
  - DSP Extensions up to 70% higher performance Audio and DSP
  - Jazelle up to 8x performance for Java (ECM)
  - Media Extensions 2x – 4x performance for audio and video
- Preserve software investment through compatibility

ARM IP Models

- ARM® provides a family of models of ARM IP suitable for a range of simulation environments. Each model provides a functional representation of a hardware component in the form of software which can be included into your chosen simulator.
- The benefits of choosing ARM models are:
  - Validated models of ARM IP
  - Broad range of third-party tool support
  - State-of-the-art modeling technology
  - Consistent views of ARM IP from specification to implementation
  - Support for hardware and software design
- The following models are also available directly from ARM:
  - Design Simulation Model (DSM)
  - Cycle-Callable Model (CCM)
  - RealView® ARMulator® ISS
  - RealView Model Library consisting of:
    - Architectural SystemC Models
    - Micro-architectural SystemC Models
    - Mirco-architectural RTL Models

ARM Architecture v4

- ARMv4

  The oldest version of the architecture supported today. All previous versions are now obsolete. Implementations include some members of the ARM7™ core family and Intel StrongARM® processors. ARMv4 can be considered a 32-bit ISA operating in a 32-bit address space.

- ARMv4T

  The ARMv4T architecture added the 16-bit Thumb instruction set which enabled compilers to generate more compact code (memory savings of up to 35% over the equivalent 32-bit code), while retaining all the benefits of a 32-bit system.

ARM Architecture v5

- ARMv5TE

  In 1999, the ARMv5TE architecture introduced improvements to the Thumb architecture, along with ARM 'Enhanced' DSP instruction set extensions to the ARM ISA.

  The Thumb changes added a few new instructions along with improvements to Thumb/ARM interworking, greatly improving compiler capabilities and the ability to mix and match ARM versus Thumb routines to balance code size and performance.

  The enhanced DSP instructions include support for saturated arithmetic, and provide up to 70% performance improvement for audio DSP applications. Many systems require the flexibility of a microcontroller combined with the data-processing capability of a DSP, historically forcing designers to compromise performance with cost, or adopt complex multi processor strategies. The 'E' instruction set extensions were designed to provide a DSP capability in a general purpose CPU, resulting in improved performance and flexibility.

- ARMv5TEJ

  In 2000, the ARMv5TEJ architecture added the Jazelle extension to support Java acceleration technology, which is particularly suited to small memory footprint designs. Jazelle technology's acceleration of Java bytecodes provides significantly higher performance than a software-only based Java Virtual Machine (JVM), accelerating Java execution by 8x and providing an 80% reduction in power consumption compared to a non Java-accelerated core. This functionality gives platform developers increased freedom to run Java code alongside established operating systems (OS) and applications on an ARM core.

Arm Architecture v6

- ARMv6

  The ARMv6 architecture, announced in 2001, features improvements in many areas covering the memory system, improved exception handling and better support for multiprocessing environments. ARMv6 also includes media instructions to support Single Instruction Multiple Data(SIMD) software execution. The SIMD extensions are optimized for a broad range of software applications including video and audio codecs, where the extensions increase performance by up to four times.

  The first implementation of the ARMv6 architecture is the ARM1136J(F)-S TM core announced in Spring 2002.

Other ARM Technologies – VFP

- Vector Floating Point (VFP)

  Vector Floating Point (VFP) coprocessor support is an architecture option. The VFP architecture supports single and double precision floating point arithmetic, and is fully IEEE 754 compliant with suitable software library support. The VFP architecture also includes a fully deterministic 'Run fast Mode'.

  Provision of a hardware floating point is essential for many applications, and can be used as part of a SoC design flow using technical computing tools (eg MatLab® and MATRIXx®) to directly model the system and derive the application code. The vector processing capability of the ARM VFP can be used to increase performance of imaging applications such as scaling, 2D and 3D transforms, font generation, and digital filters.

  ARM currently has VFP support for the ARM9™, ARM10™ and ARM11™ processor families: VFP9-S ™ and VFP10™

Other ARM Technologies – Trustzone

ARM TrustZone

The ARM TrustZone extensions provide hardware support for two separate address spaces, such that code executing in the non-secure world cannot gain access to any address space marked as secure. A new monitor mode supports transition between the two worlds.

The technology provides a secure environment for system features such as key management and/or authentication mechanisms enabled by an open OS. The protection provided by the technology is necessary for consumer privacy and extending a range of services, such as mobile banking and multimedia entertainment, to widespread consumer adoption and use

Other ARM Technologies – Thumb2

Thumb-2 Core Technology

ARM and Thumb code each execute in their own processor state. Thumb-2 core technology adds a mixed mode capability, defining a new set of 32-bit instructions that execute alongside traditional 16-bit instructions in Thumb state. This reduces, or can remove, the need for balancing ARM and Thumb code in a system, providing 'ARM levels of performance' with 'Thumb code density'.

Thumb-2 core technology builds on the success of Thumb technology, adding to ARM's strengths as the leading supplier of low power, high performance processors and systems, supply cost effective and timely solutions across a wide range of market segments.

ARM PrimeCells

- ARM PrimeCell Peripherals are re-usable soft IP macrocells developed to enable the rapid assembly of System-on-Chip (SoC) designs. Ready to use, fully verified and compliant with the AMBA on chip bus standard, the ARM PrimeCell range is designed to provide right first time functionality and high system performance.
- PrimeCell AXI Level-2 Cache Controller (L220)
- PrimeCell AXI Configurable Interconnect (PL300)
- PrimeCell AXI SDRAM Controller (PL340)

Other ARM Technologies – VFP

- Debug and Trace

  ARM's debug and trace tools enable system developers to quickly debug realtime software, and to trace instruction execution and associated program data at full core speed. The debug and trace offering includes host based tools along with components such as EmbeddedICE, Embedded Trace Macrocell™ (ETM™), and the latest CoreSight™ technology, which form part of a modern SoC.

- AMBA TM

  The AMBA on-chip interconnect is an established, open specification that serves as framework for SoC designs and IP library development. The AMBA Advanced High-performance Bus (AHB) interface is supported by all many ARM cores and provides a high-performance, fully-synchronous backplane. Multi-layer AHB represents a significant technical advance that reduces latencies and increases the bandwidth available to multi-master systems. Fully compatible with the current AHB specification, Multi-layer AHB is supported on the ARM926EJ-S™ core and by all members of the ARM10™ core family. In 2003, ARM announced the launch of the latest AMBA specification, AMBA AXI which is targeted at high performance, high clock frequency systems designs and includes a number of features that make it very suitable for high speed, submicron interconnect.

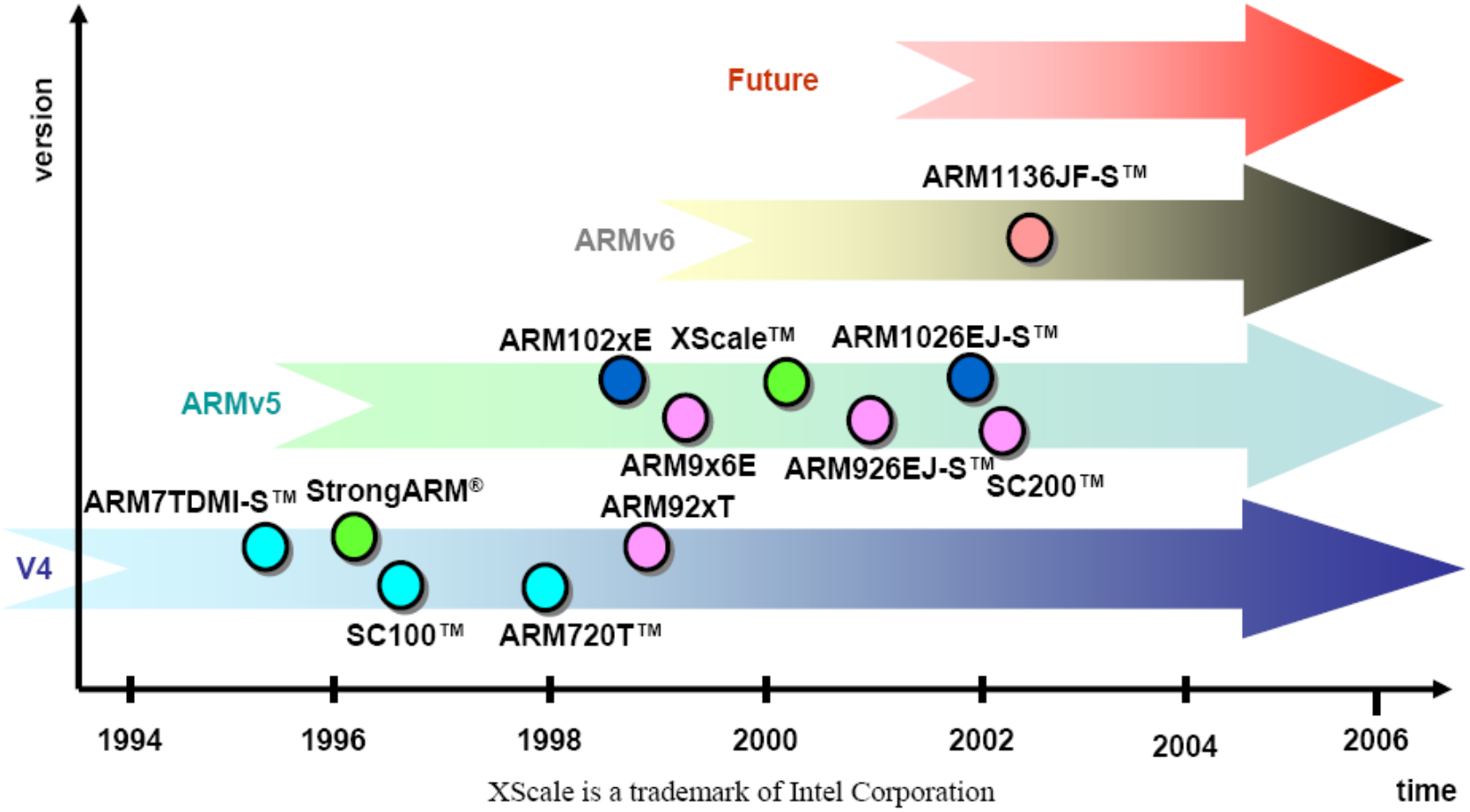
Other ARM Technologies – IEM

- ARM Intelligent Energy Manager

  ARM Intelligent Energy Manager (IEM) technology implements advanced algorithms to optimally balance processor workload and energy consumption, while maximizing system responsiveness to meet end-user performance expectations. The Intelligent Energy Manager technology works with the OS and applications running on the mobile phone to dynamically adjust the required CPU performance level through a standard programmer's model.

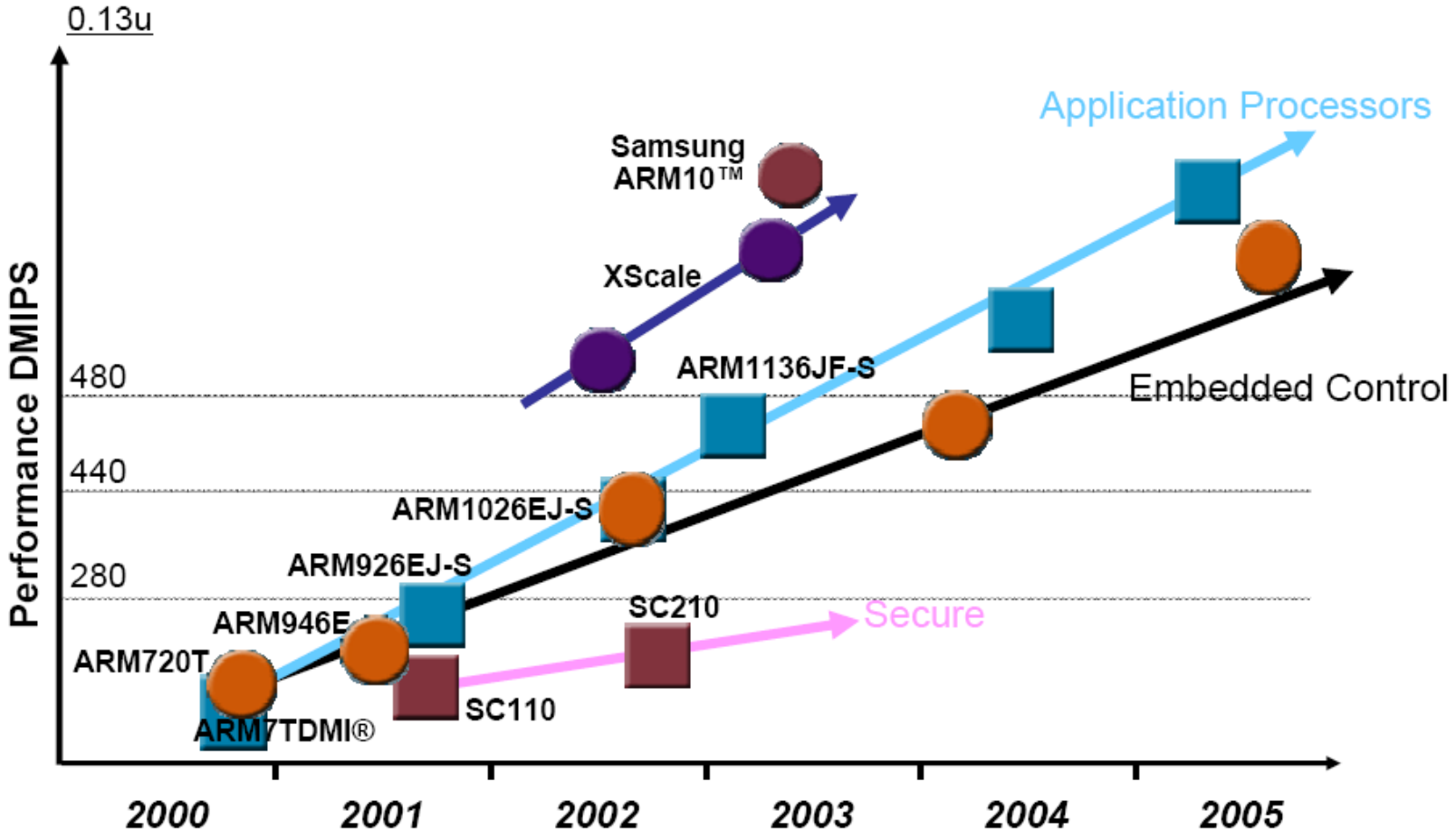
	Cache Size (Inst/Data)	Tightly Coupled Memory	Memory Mgt	Bus Interface	Thumb	DSP	Jazelle
APPLICATION CORES							
ARM1020E	32k/32k	-	MMU	2x AHB	Yes	Yes	No
ARM1022E	16k/16k	-	MMU	2x AHB	Yes	Yes	No
ARM1026EJ-S	Variable	Yes	MMU or MPU	2x AHB	Yes	Yes	Yes
ARM1136J(F)-S	Variable	Yes	MMU	5x AHB	Yes	Yes	Yes
ARM1176JZ(F)-S	Variable	Yes	MMU + TrustZone	4x AXI	Yes	Yes	Yes
ARM720T	8k unified	-	MMU	AHB	Yes	No	No
ARM920T	16k/16k	-	MMU	ASB	Yes	No	No
ARM922T	8k/8k	-	MMU	ASB	Yes	No	No
ARM926EJ-S	Variable	Yes	MMU	2x AHB	Yes	Yes	Yes
MPCore Multiprocessor Core	Variable	-	MMU + cache coherency	1x or 2x AMBA AXI	Yes	Yes	Yes
EMBEDDED CORES							
ARM1026EJ-S	Variable	Yes	MMU or MPU	2x AHB	Yes	Yes	Yes
ARM1156T2(F)-S	Variable	Yes	MPU	4xAXI	Yes	Yes	No
ARM7EJ-S	-	-	-	Yes	Yes	Yes	Yes
ARM7TDMI	-	-	-	Yes**	Yes	No	No
ARM7TDMI-S	-	-	-	Yes	Yes	No	No
ARM940T	Fixed	-	MPU	ASB	Yes	No	No
ARM946E-S	Variable	Yes	MPU	AHB	Yes	Yes	No
ARM966E-S	-	Yes	-	AHB	Yes	Yes	No
ARM968E-S		Yes	DMA	AHB-Lite	Yes	Yes	No
SECURE APPLICATIONS							
SecurCore SC100	-	-	MPU	-	Yes	No	No
SecurCore SC110	-	-	MPU	-	Yes	No	No
SecurCore SC200	-	-	MPU	-	Yes	Yes	Yes
SecurCore SC210	-	-	MPU	-	Yes	Yes	Yes

Architecture Revisions

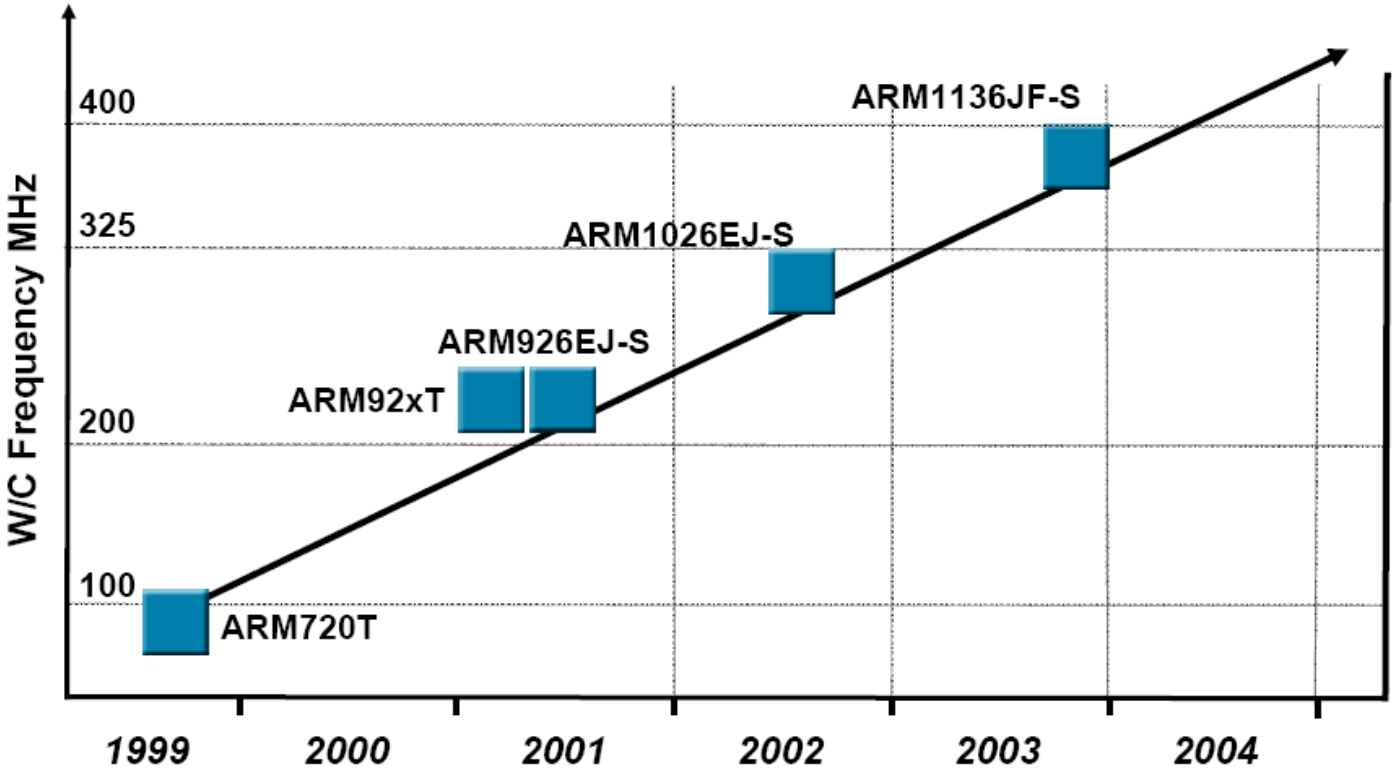


XScale is a trademark of Intel Corporation

ARM CPU Roadmap

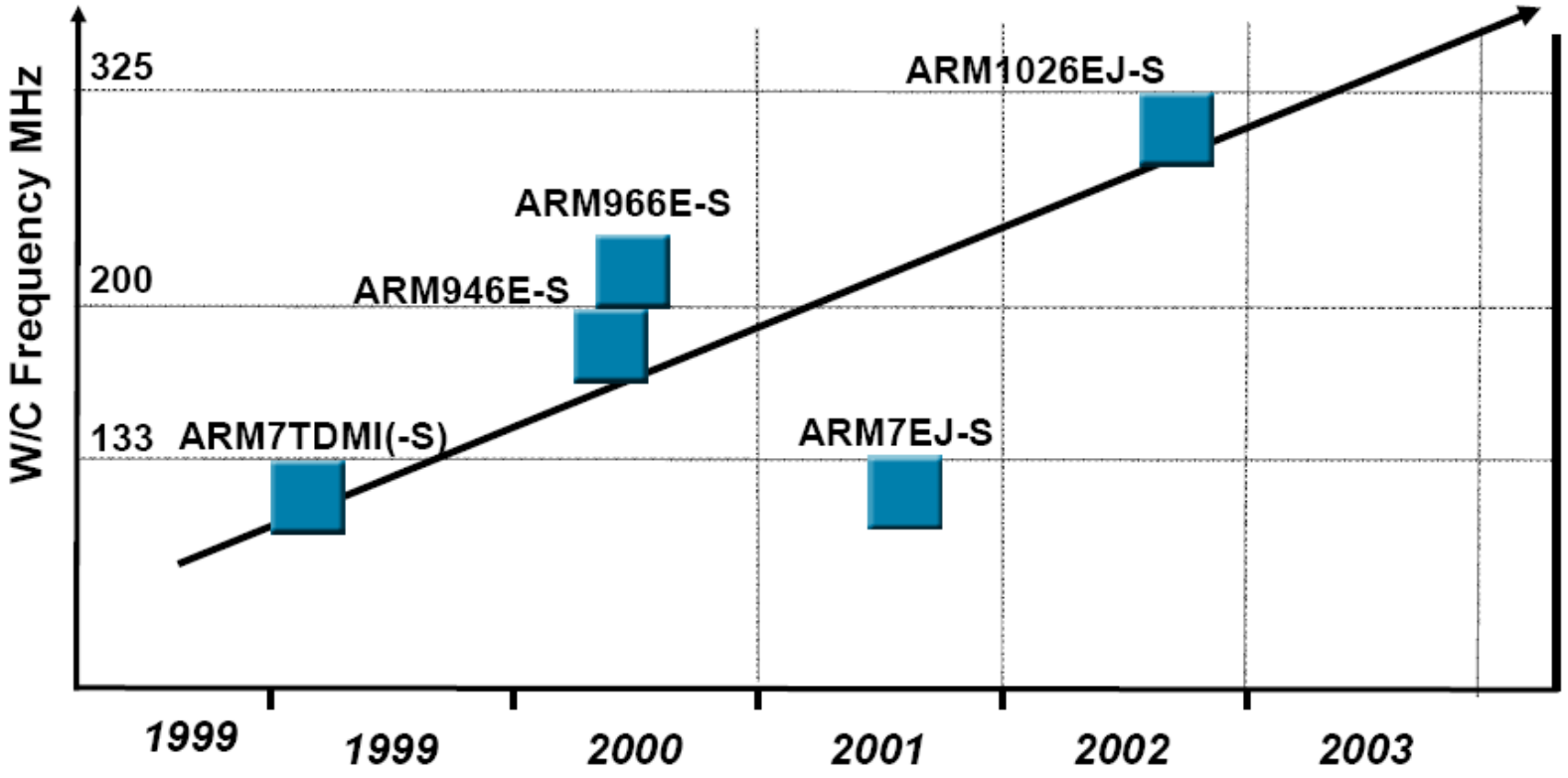


Application Processors



0.13u generic foundry process, 1.08V, 125degC, slow silicon, average port & synthesis & cell library

Embedded Control Processors



0.13u generic foundry process, 1.08V, 125degC, slow silicon, average port & synthesis & cell library

ARM7 Family

The ARM7 family is a range of low-power 32-bit RISC microprocessor cores optimized for cost and power-sensitive consumer applications.

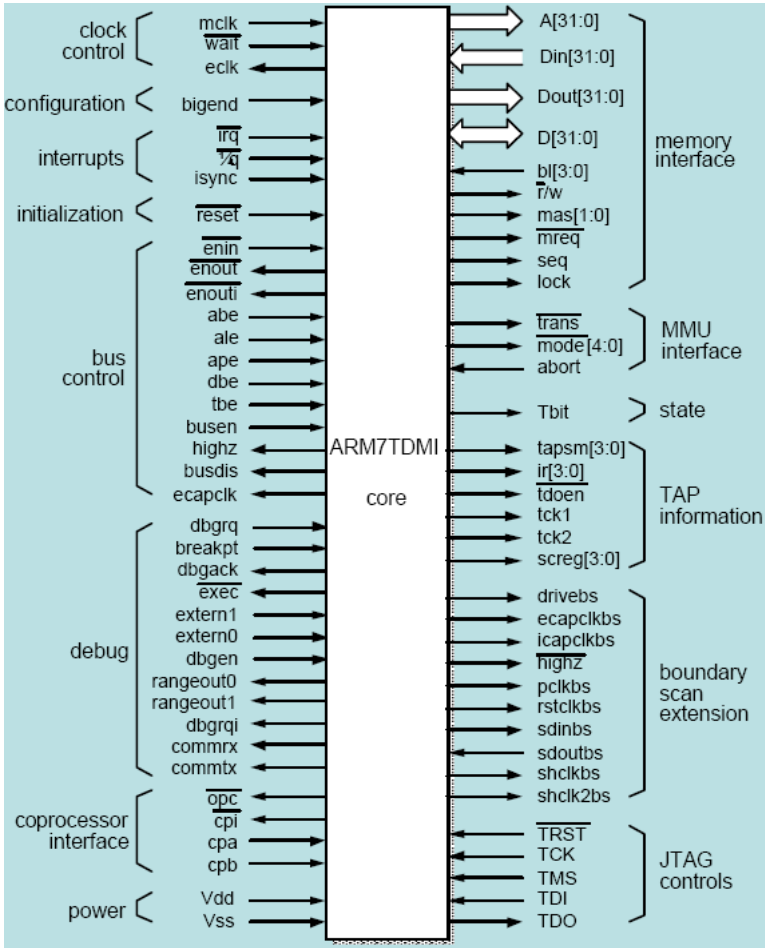
- Von Neuman Architecture
- 3 stage pipeline
- CPI ≈ 1.2
- Established, high-volume 32-bit RISC architecture
- Up to 130 MIPs (Dhrystone 2.1) performance on a typical 0.13µm process
- Small die size and very low power consumption
- High code density, comparable to 16-bit microcontroller
- Wide operating system and RTOS support – including Windows CE, Palm OS, Symbian OS, Linux and market-leading RTOS
- Wide choice of development tools
- Simulation models for leading EDA environments
- Excellent debug support for SoC designers, including ETM interface
- Multiple sourcing from industry-leading silicon vendors
- Availability in 0.25µm, 0.18µm and 0.13µm processes
- Migration and support across new process technologies
- Code is forward-compatible to ARM9, ARM9E and ARM10 processors as well as Intel's XScale technology

• Applications:

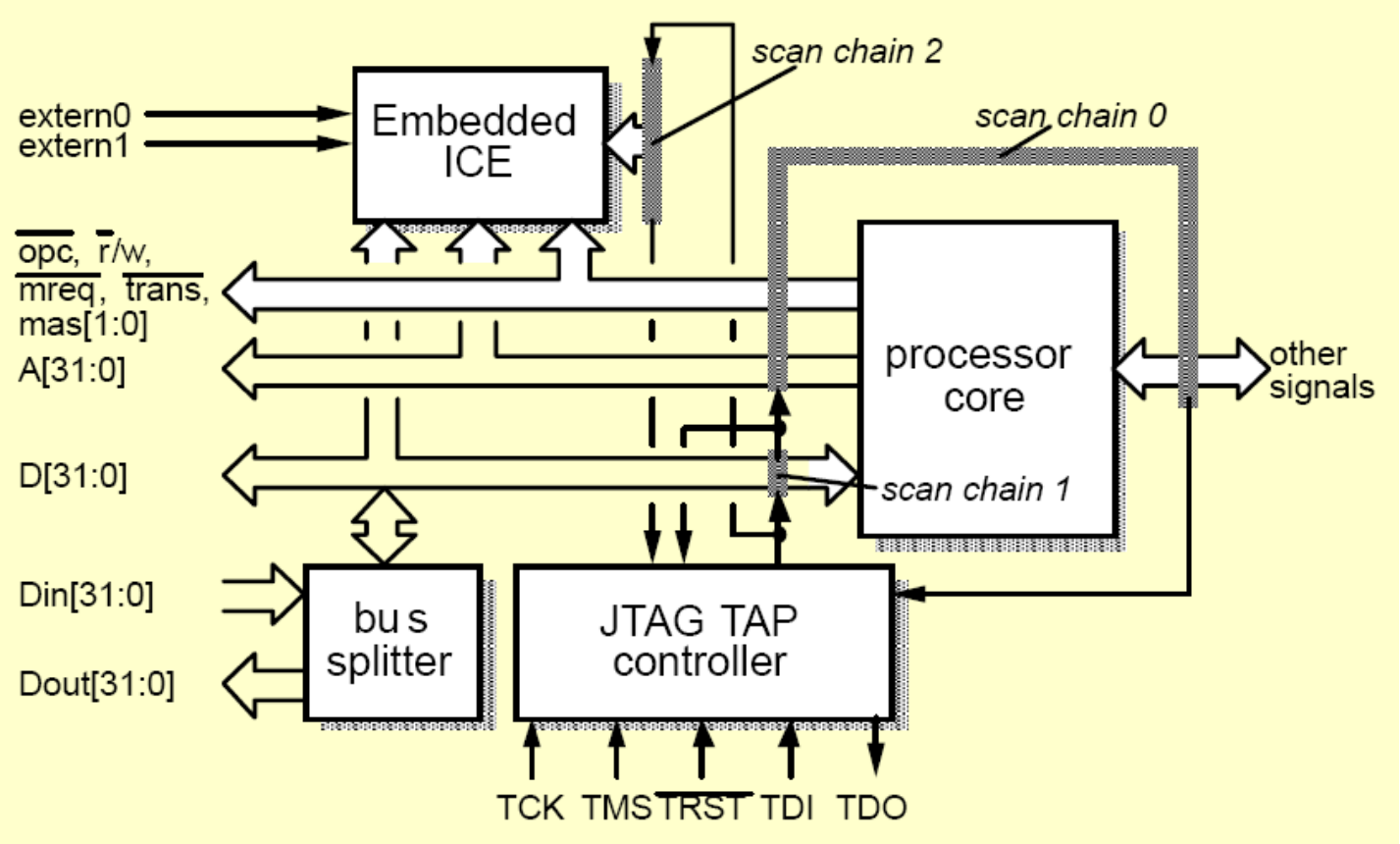
- Personal audio (MP3, WMA, AAC players)
- Entry level wireless handsets
- Two-way pagers

ARM7TDMI core interface signals

- Read the book for more info

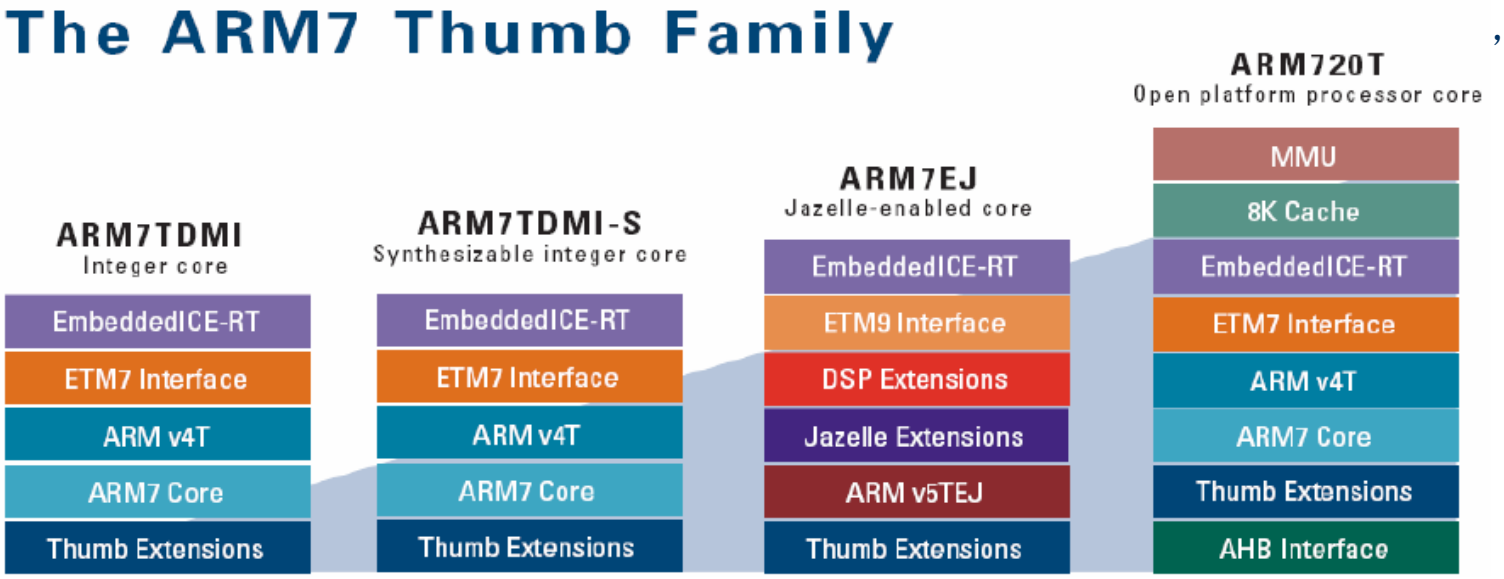


ARM7TDMI Organization



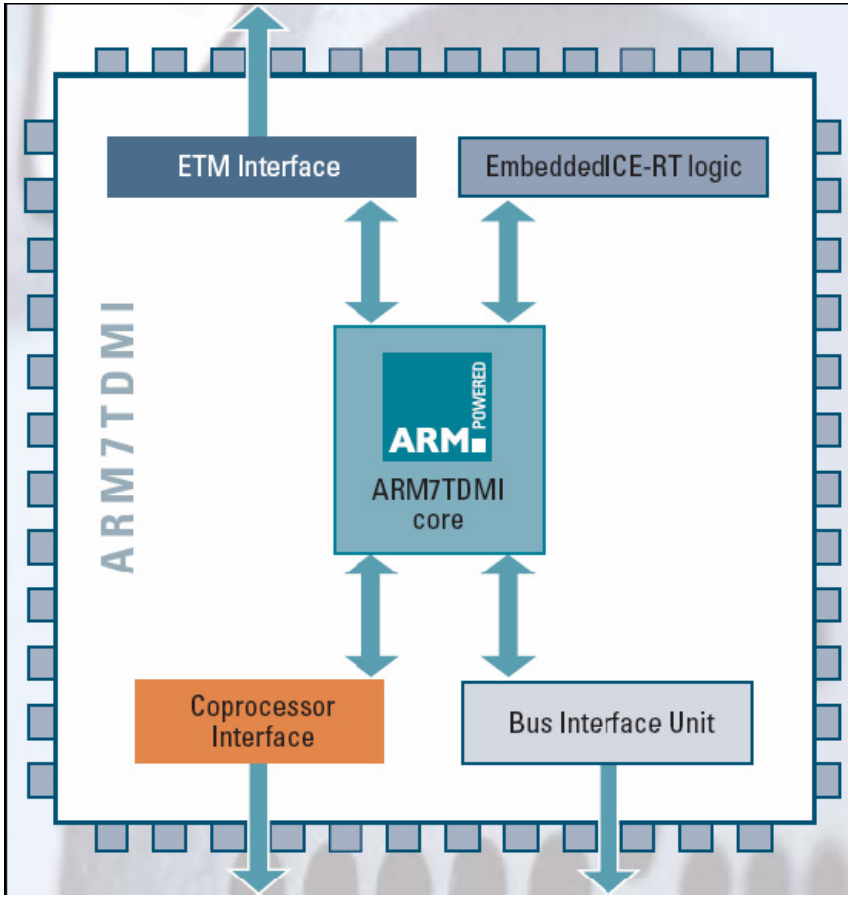
ARM7 Cores

- ARM7TDMI: Integer core
- ARM7TDMI-S: Synthesizable version of the ARM7TDMI core
- ARM7EJ-S: Synthesizable core with DSP and Jazelle TM technology enhancements for Java acceleration
- ARM720T: Cached core with Memory Management Unit (MMU)



ARM7TDMI

- The ARM7TDMI core is the industry's most widely used 32-bit embedded RISC microprocessor.
- Optimized for cost and power sensitive applications
- Key features are:
  - Hard macrocell
  - Portable down to 0.13µm
  - Performance up to 120 MIPS (Dhrystone 2.1)
  - Thumb and ARM instruction sets
  - Three-stage pipeline
  - Unified bus architecture
  - Low power, fully static design
  - Small die size
  - Coprocessor interface
  - EmbeddedICE-RT™ debug logic
  - Embedded Trace Macrocell™ (ETM) interface

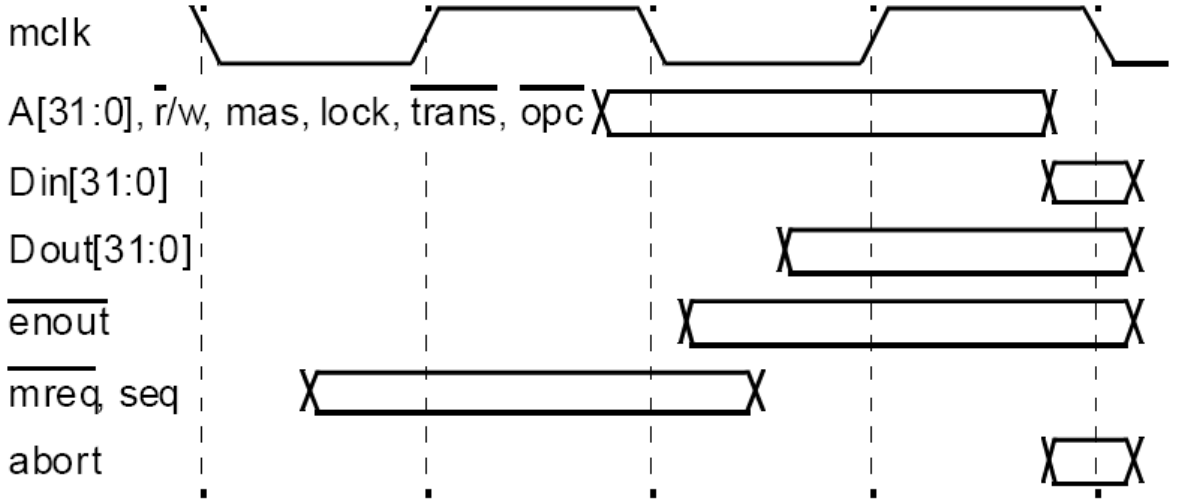


ARM7TDMI Memory Interface

- ARM7 Memory cycle types

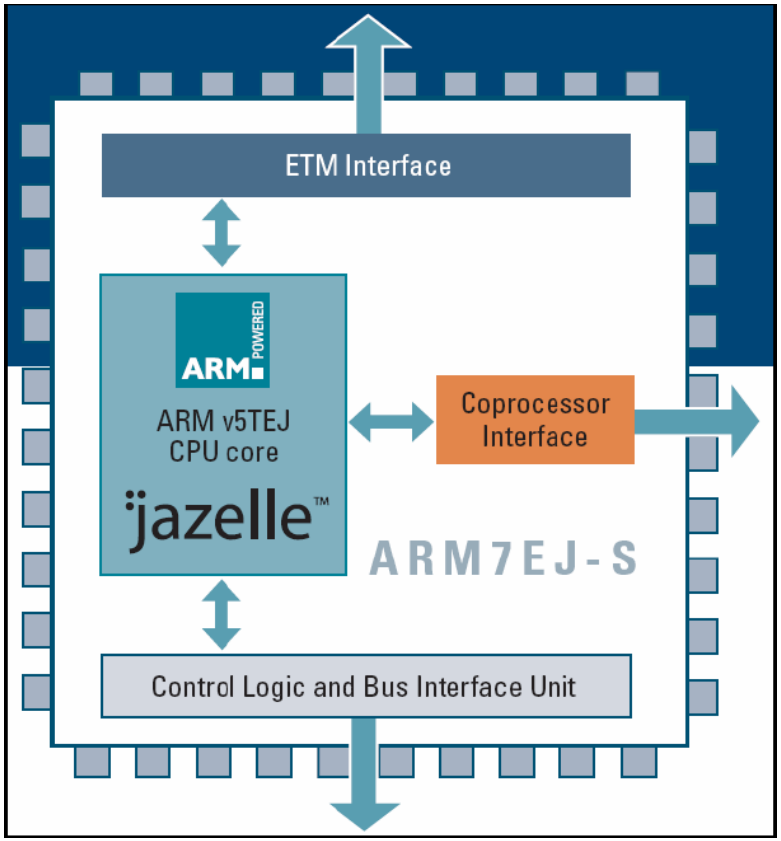
mreq	seq	Cycle	Use
0	0	N	Non-sequential memory access
0	1	S	Sequential memory access
1	0	I	Internal cycle – bus and memory inactive
1	1	C	Coprocessor register transfer – memory inactive

- ARM7TDMI core memory and MMU interface timing



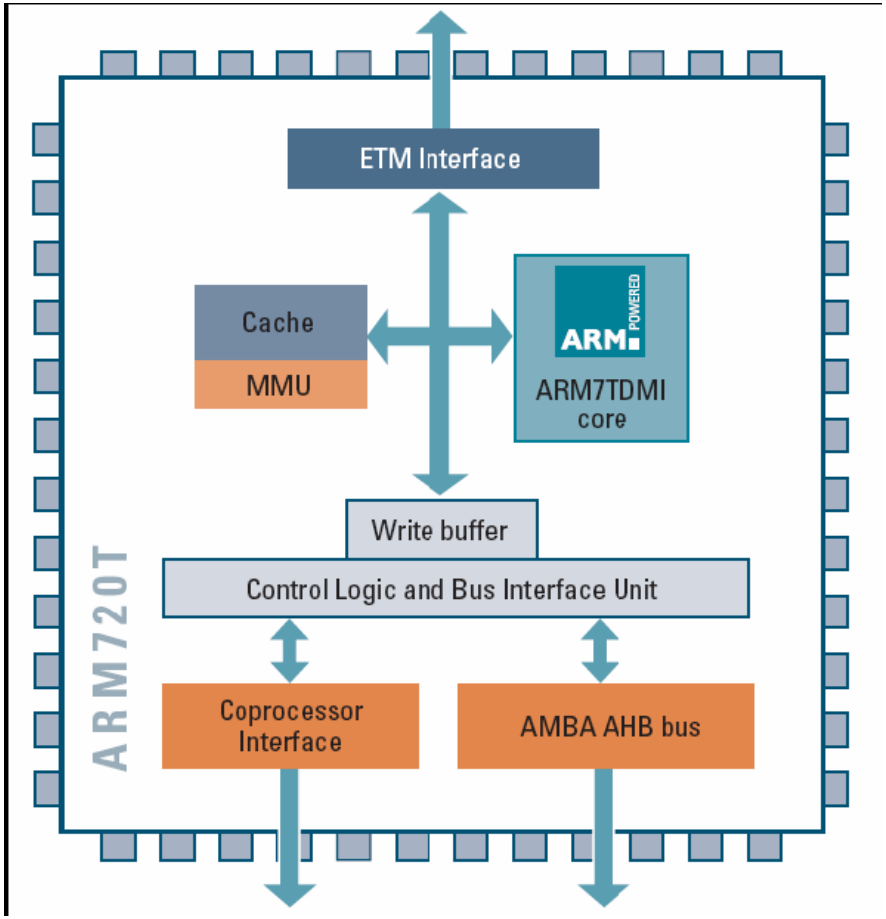
ARM7JE-S

- The ARM7EJ-S core provides all the benefits of the ARM7TDMI core plus ARM's Jazelle technology and DSP extensions
- Typical perfomance is up to 120 MIPS on a typical 0.13µm process (Dhrystone2.1).
- Jazelle Technology
  - ARM's Jazelle technology provides hardware acceleration to deliver up to 8 times higher Java performance compared to a software-only Java Virtual Machine (JVM).
  - Jazelle technology-enabled ARM cores also use over 80% less energy per CaffeineMark than an equivalent nonaccelerated ARM core. Because Jazelle extends the ARM7 core functionality, developers have the freedom to run Java code alongside existing operating systems and applications offering a fast upgrade path for designs using the ARM7TDMI core.
- DSP Instructions
  - The ARM7EJ-S processor incorporates the ARM DSP extensions that offer enhanced 16-bit and 32-bit arithmetic capabilities within the functionality of a CPU, for improved performance and flexibility.
  - Key features are:
    - 16-bit data operations
    - Saturating, signed arithmetic — on both 16-bit and
    - 32-bit data
    - Enhanced MAC operations.

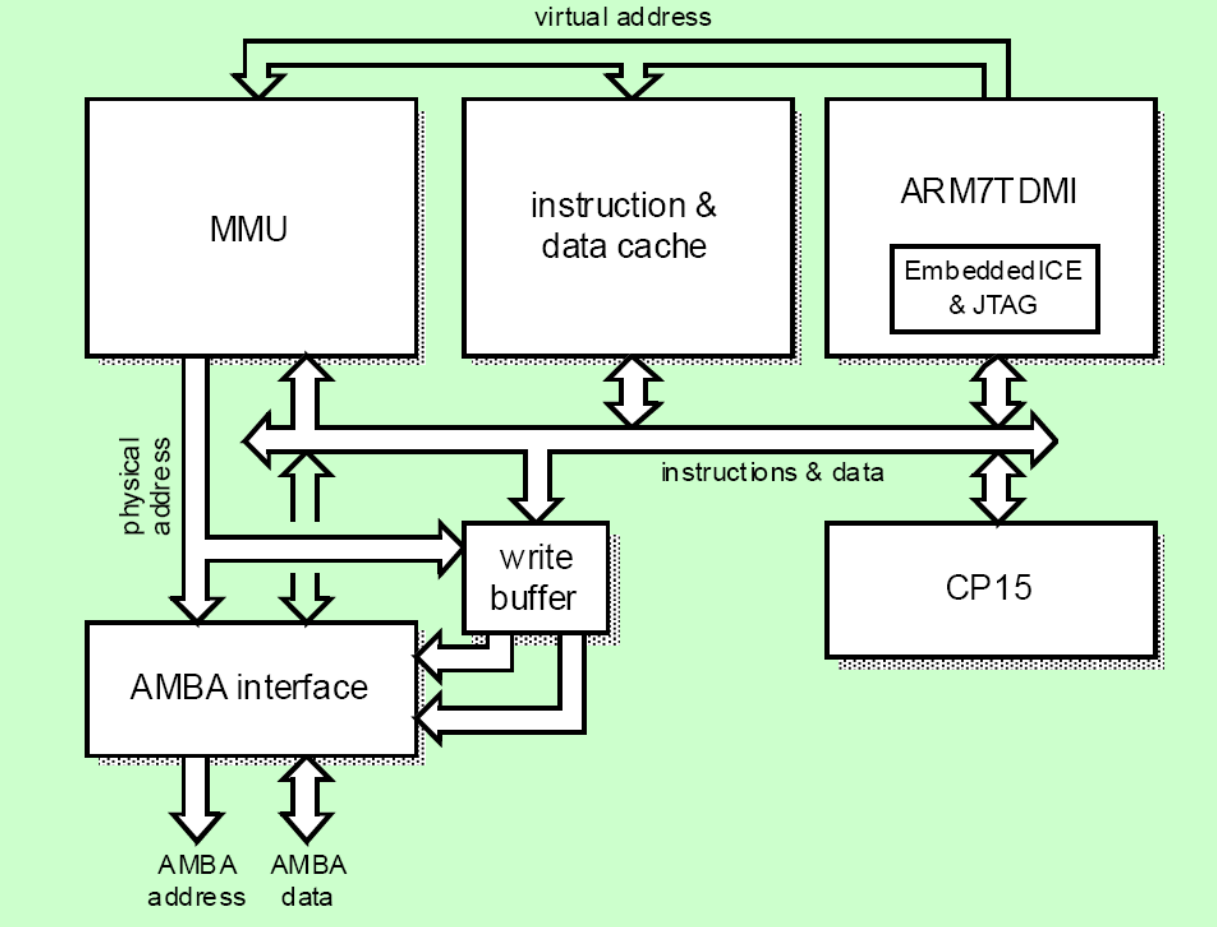


ARM720T Macrocell

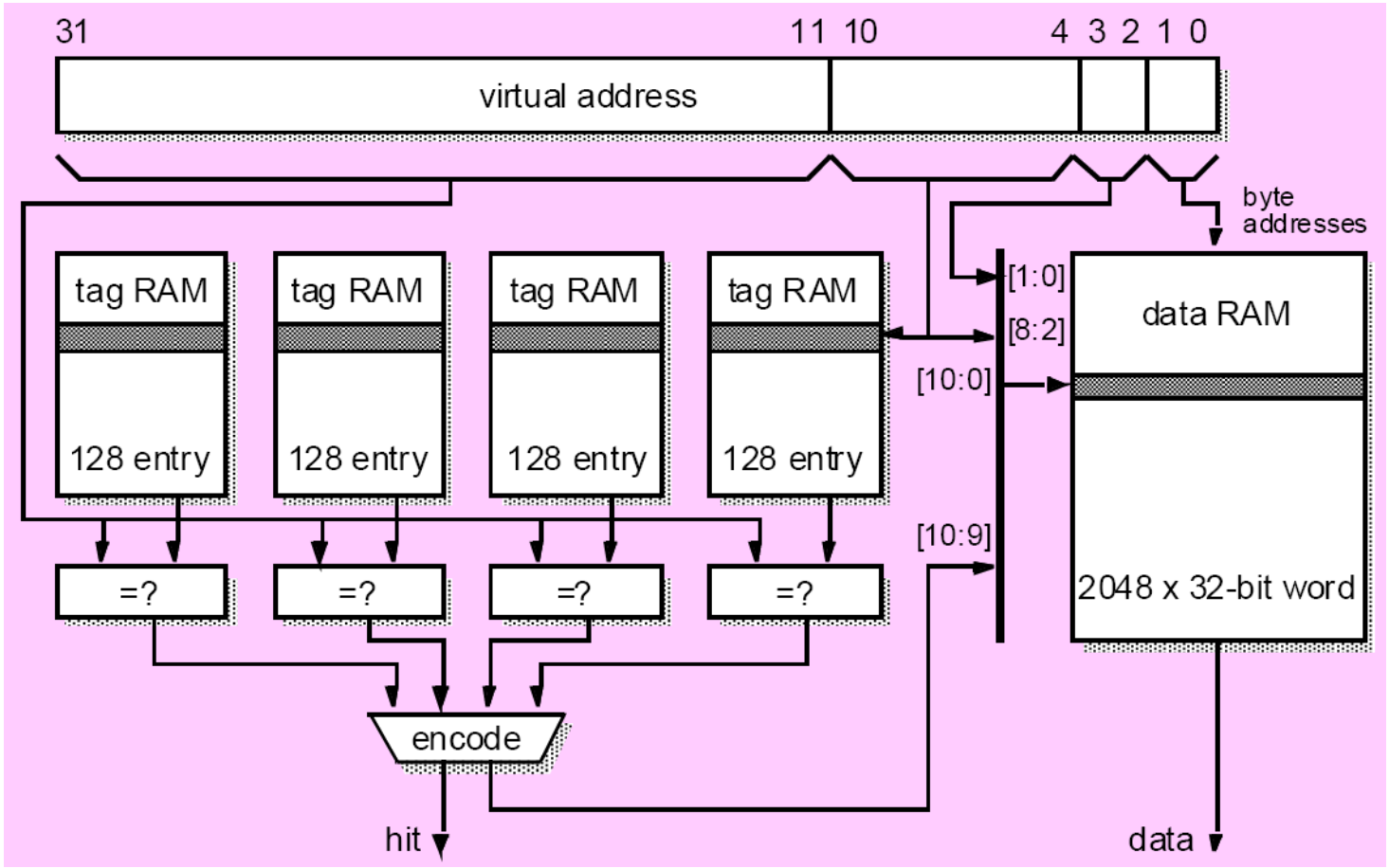
- The ARM720T hard macrocell is a high performance processor for systems requiring full virtual memory management and protected execution spaces. It is compatible with leading operating systems such as Linux, Palm OS, Symbian OS and Windows CE.
  - It combines the ARM7TDMI core with:
  - 8K unified cache
  - Memory Management Unit (MMU)
  - Write buffer
  - AMBA AHB bus interface
- The ARM720T core retains the coprocessor and ETM interfaces for system expansion and realtime debug capabilities.
- ARM720T System Benefit
- The on-chip cache and write buffer substantially raise the average execution speed and reduce the average amount of system bus bandwidth required by the processor.
- There are multiple benefits to system design:
  - The system bus and external memory can be run at lower speed than the processor, reducing power consumption
  - External memory can support additional processors or Direct Memory Access (DMA) channels with minimal performance loss.
  - Low-cost commodity RAM can be used.
- The ARM720T processor has a built-in coprocessor (CP15) which is used for internal control of cache and MMU.



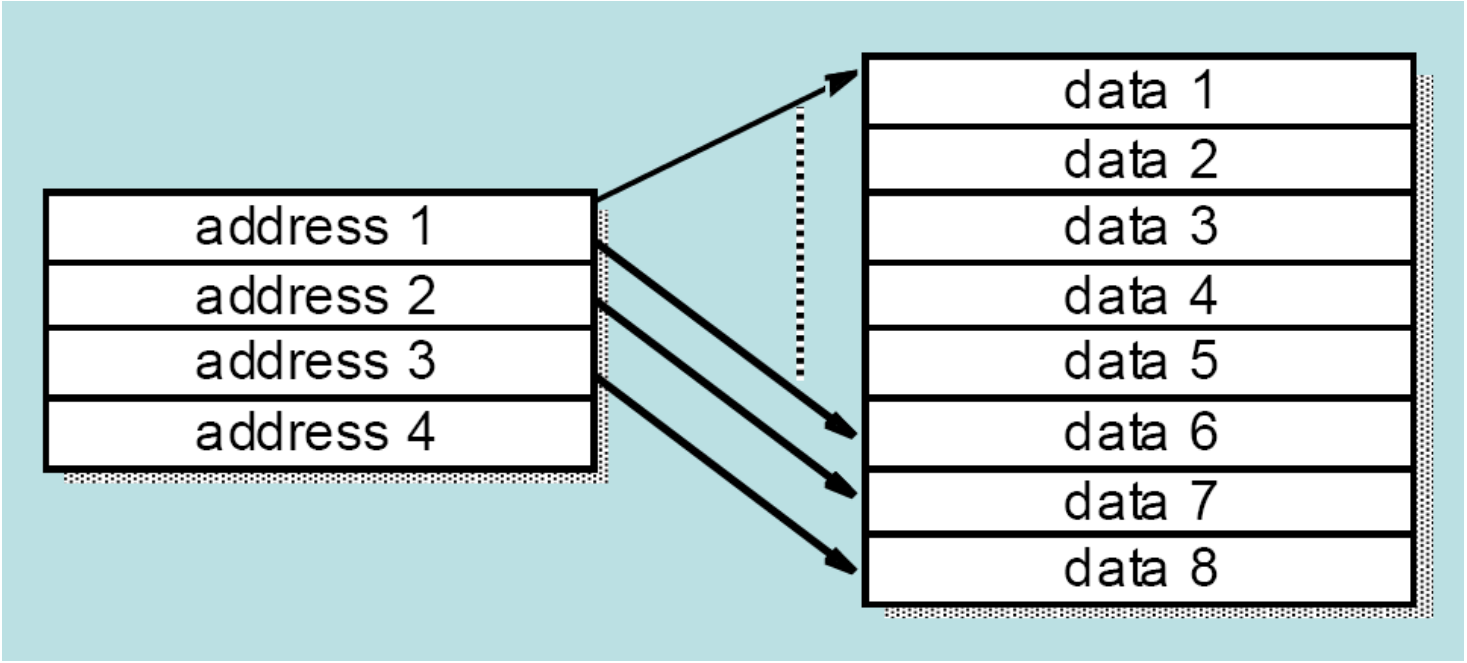
ARM710T and ARM720T Organization



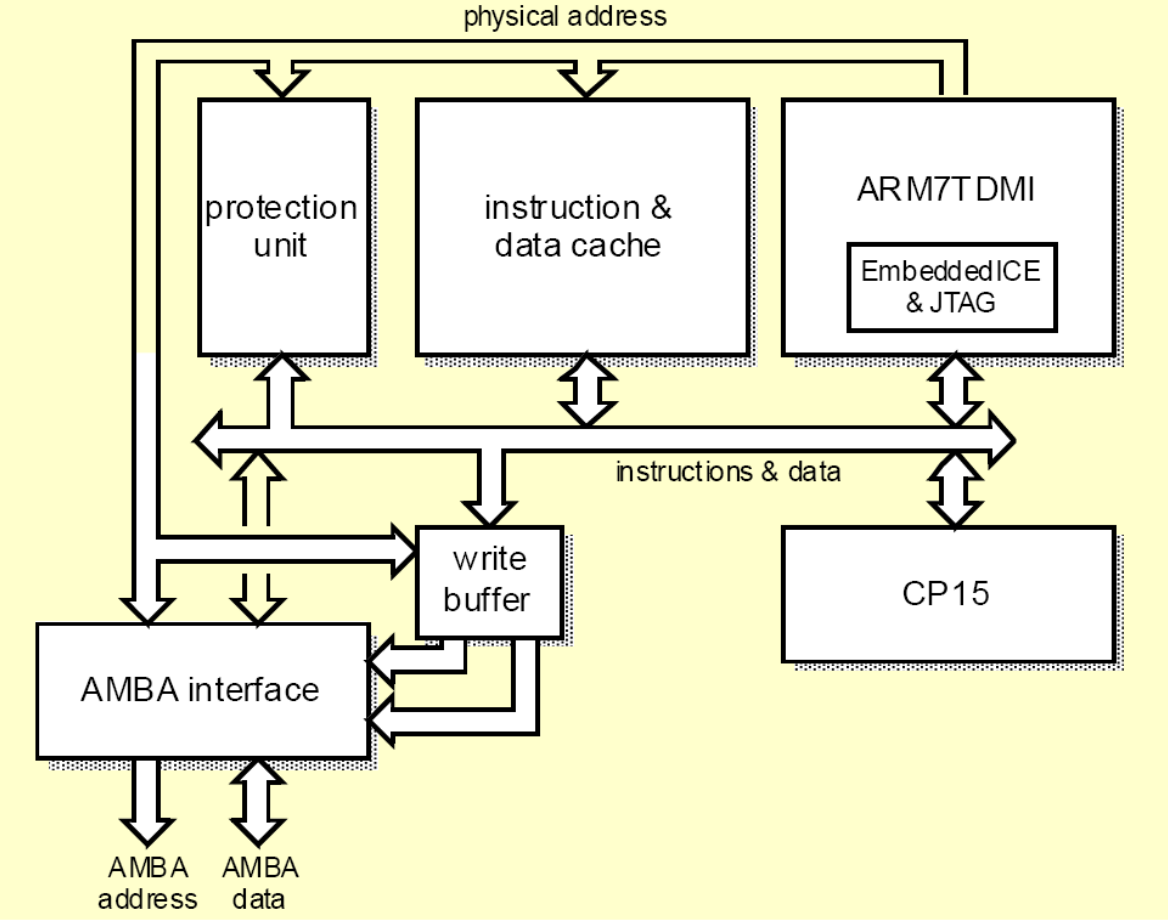
The ARM710T cache organization



Write buffer mapping example



ARM740T Organization



Comparison of ARM7 cores

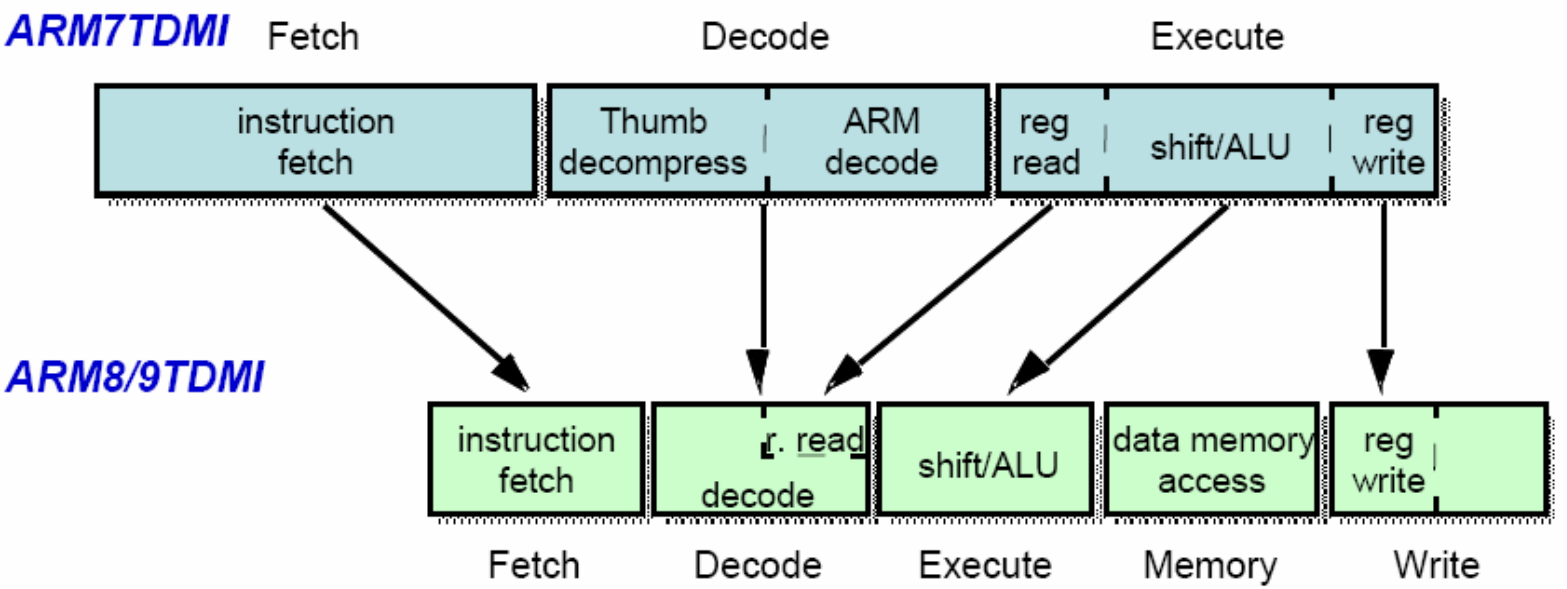
PERFORMANCE CHARACTERISTICS

Processor	Generic Foundry Process	Performance MIPS/MHz (Dhrystone 2.1)	Power Consumption mW/MHz (Typical[1])	Area mm²	Frequency MHz (Worst case[2])
ARM7TDMI	0.18µm	0.9	0.25	0.53	90
ARM7TDMI-S	0.18µm	0.9	0.39	0.62	80-110
ARM7EJ-S	0.18µm	1.0	0.45	0.95	80-110
ARM720T	0.18µm	0.9	0.65	3.00	75
ARM7TDMI	0.13µm	0.9	0.06	0.26	133
ARM7TDMI-S	0.13µm	0.9	0.10	0.32	100-133
ARM7EJ-S	0.13µm	1.0	0.18	0.42	100-133
ARM720T	0.13µm	0.9	0.20	2.40	100

[1] Typical figures on nominal silicon at 25 °C
Average port & synthesis & cell library
0.18 µm at 1.8V, 0.13 µm at 1.2V

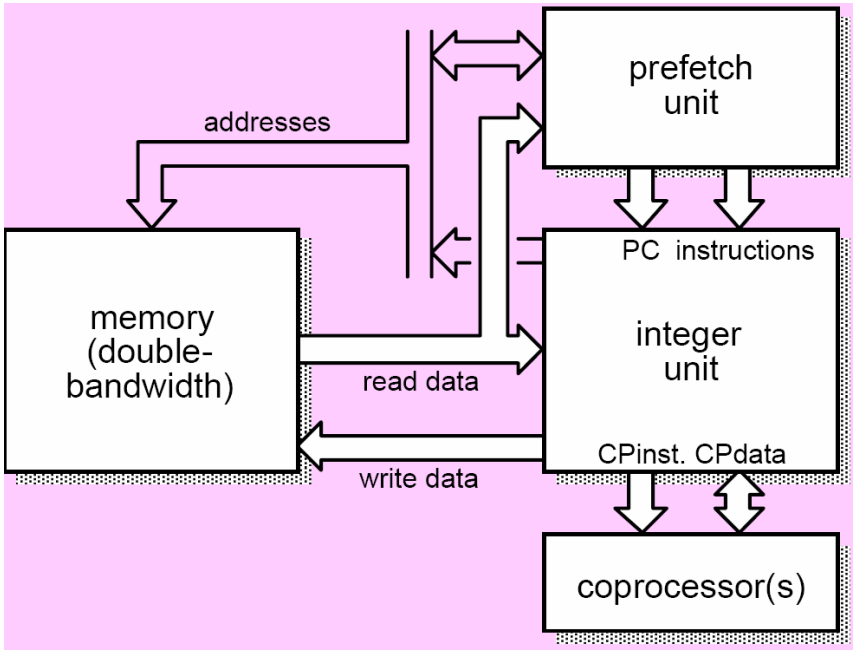
[2] Worst case figures on slow silicon at 125 °C
Average — best port & synthesis & cell library
0.18 µm at 1.62V, 0.13 µm at 1.08V

ARM7TDMI and ARM8/9TDMI pipeline comparisons

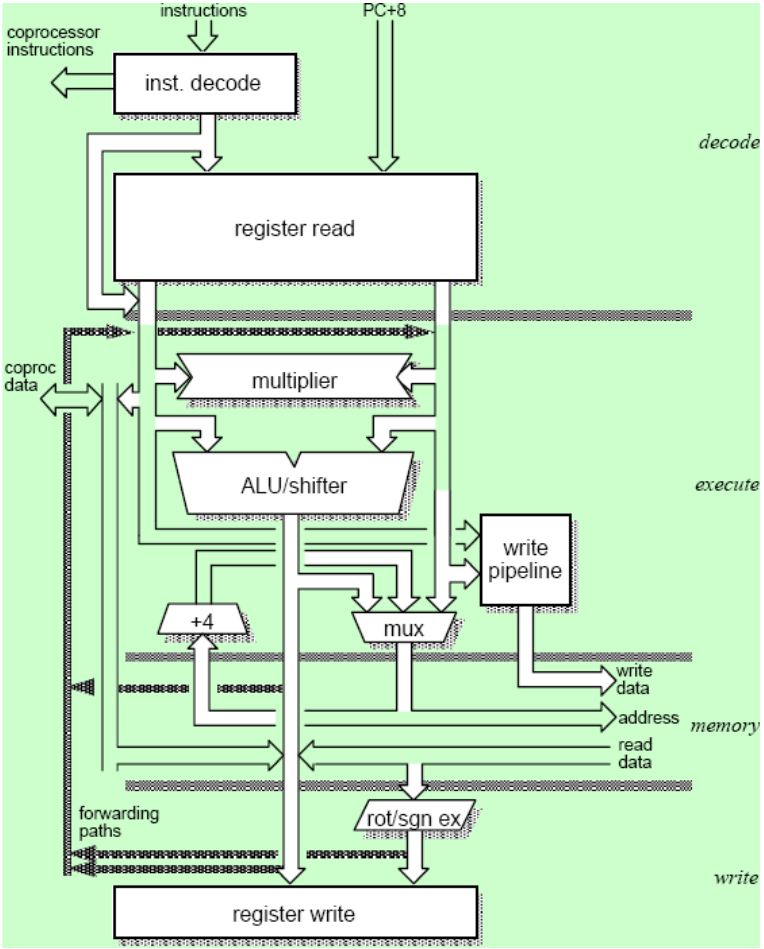


ARM8 processor core organization

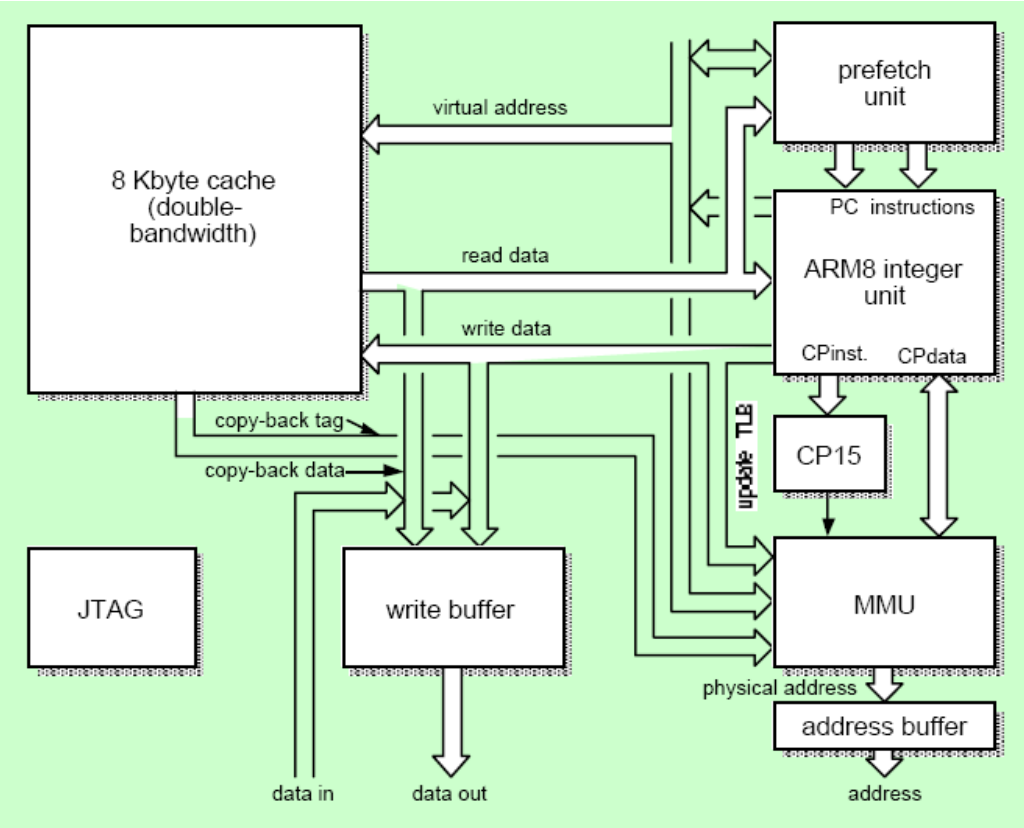
- ARM8 was an ARM experiment which did notlast long
- Maintains von-Neuman Architecture
- Uses 5-stage pipeline
- Some data-forwarding was introduced
- Mainly it is the ARM7 core with doublebandwidth memory (only good for sequential reads)



ARM8 integer unit organization

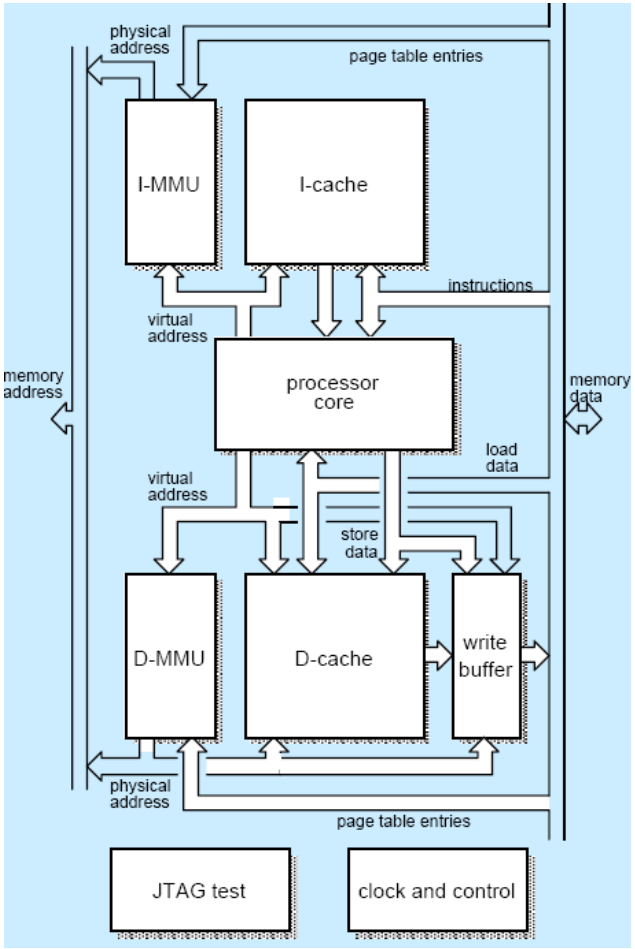


ARM810 organization

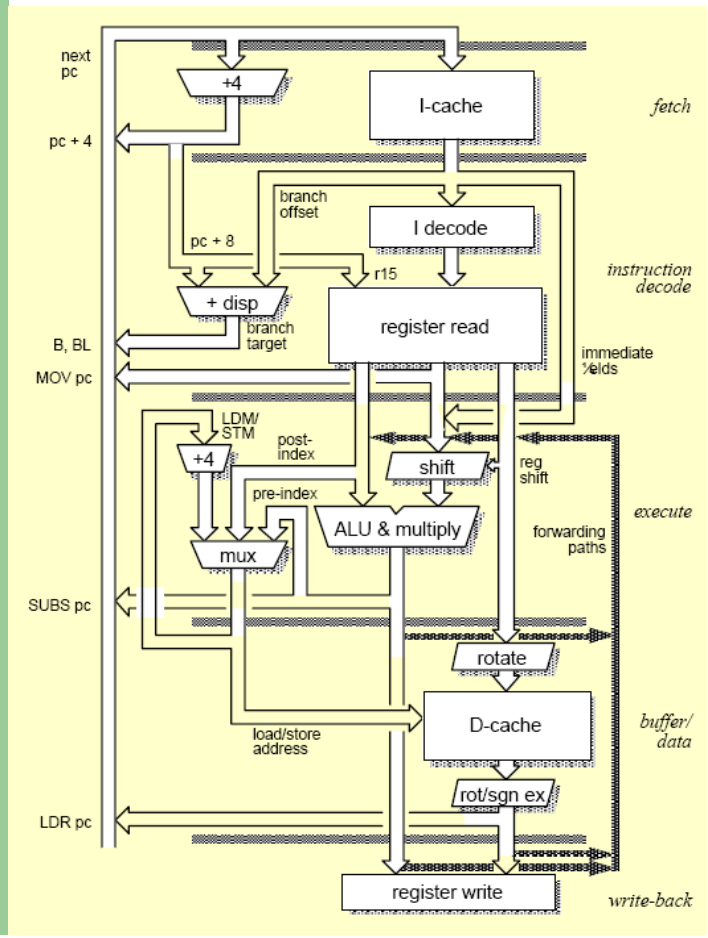


Process	0.5 um	**Transistors**	836,022	**MIPS**	86
Metal layers	3	**Die area**	76 mm^2	**Power**	500 mW
Vdd	3.3 V	**Clock**	0 to 72 MHz	**MIPS/W**	172

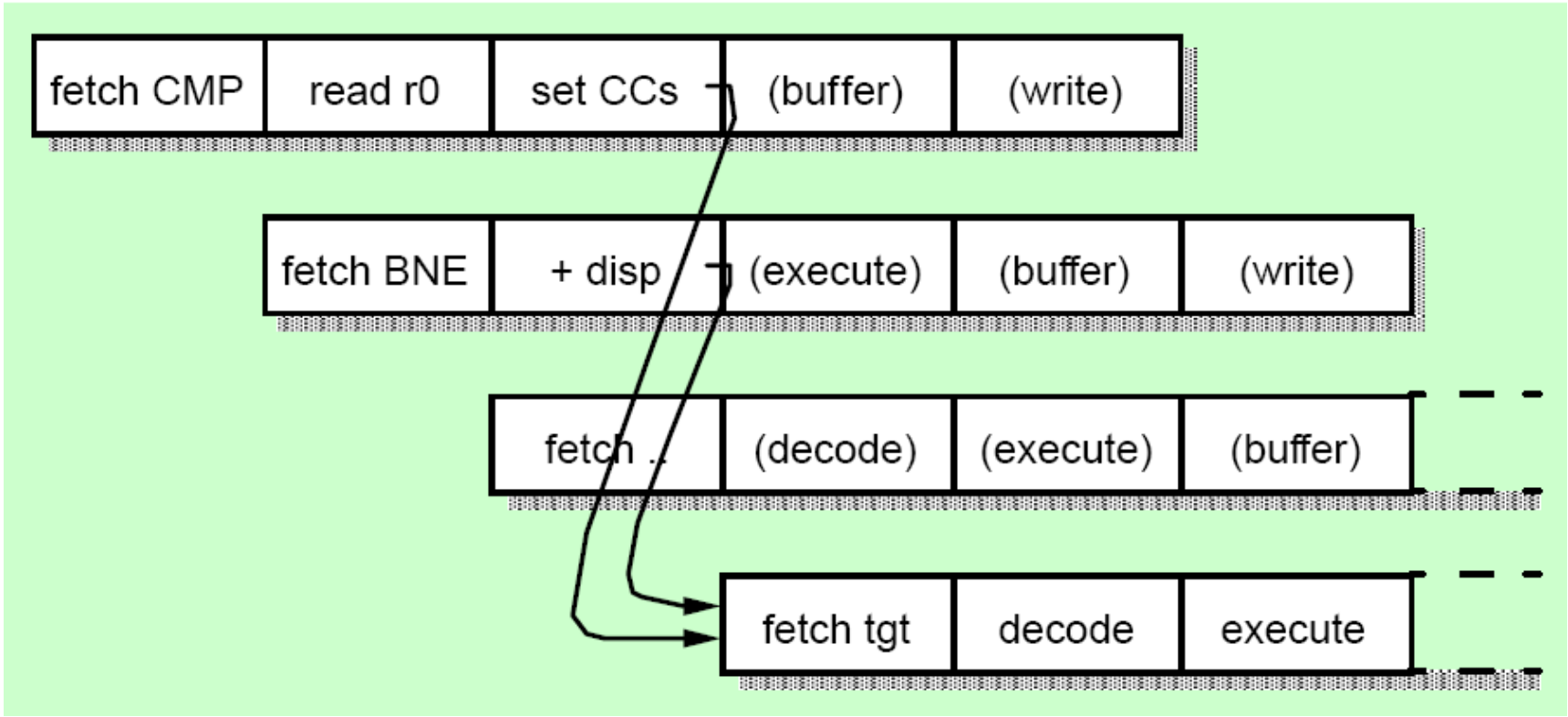
StrongARM organization



StrongARM core pipeline organization



StrongARM loop test pipeline behaviour



ARM 9 Family

- The ARM9 family is built around the ARM9TDMI processor core and incorporates the 16-bit Thumb instruction set, which improves code density by as much as 35%.
- Features
  - Harvard architecture
  - 5-stage pipeline
  - Improve CPI to ≈ 1.5
  - Improve maximum clock frequency
  - 32-bit RISC processor core with ARM® and Thumb® instruction sets
  - 5-stage integer pipeline achieves 1.1 MIPS/MHz
  - Up to 300 MIPS (Dhrystone 2.1) in a typical 0.13µm process
  - Single 32-bit AMBA bus interface
  - MMU supporting Windows CE, Symbian OS, Linux, Palm OS (ARM920T and ARM922T)
  - Memory Protection Unit (MPU) supporting a range of Real Time Operating Systems including VxWorks (ARM940T)
  - Integrated instruction and data caches
  - Excellent debug support for SoC designers, including ETM interface
  - 8-entry write buffer — avoids stalling the processor when writes to external memory are performed
  - Portable to latest 0.18µm, 0.15µm, 0.13µm silicon processes

Comparison of ARM7 and ARM9 Pipelines

Figure 1 : The ARM7TDMI core and ARM7TDMI-S core pipeline

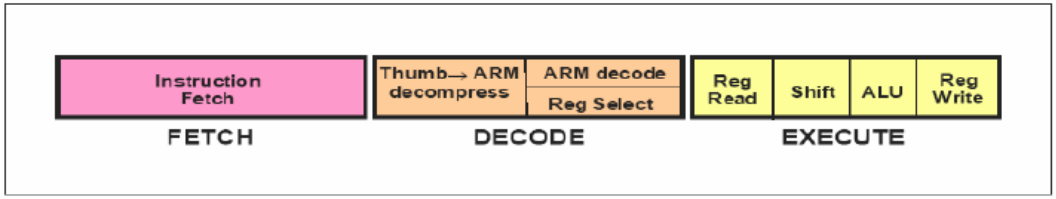


Figure 2 : The ARM9TDMI core pipeline

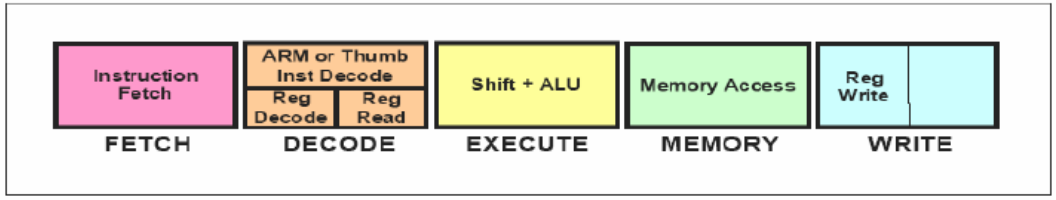
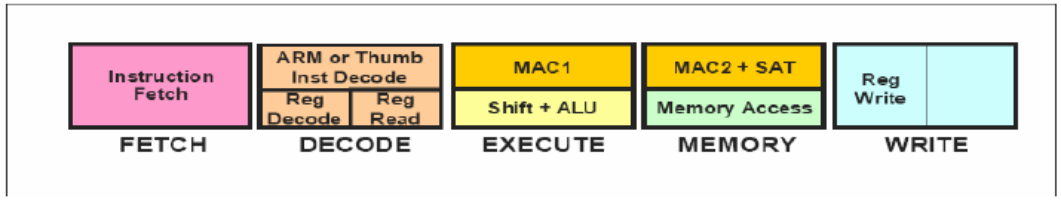
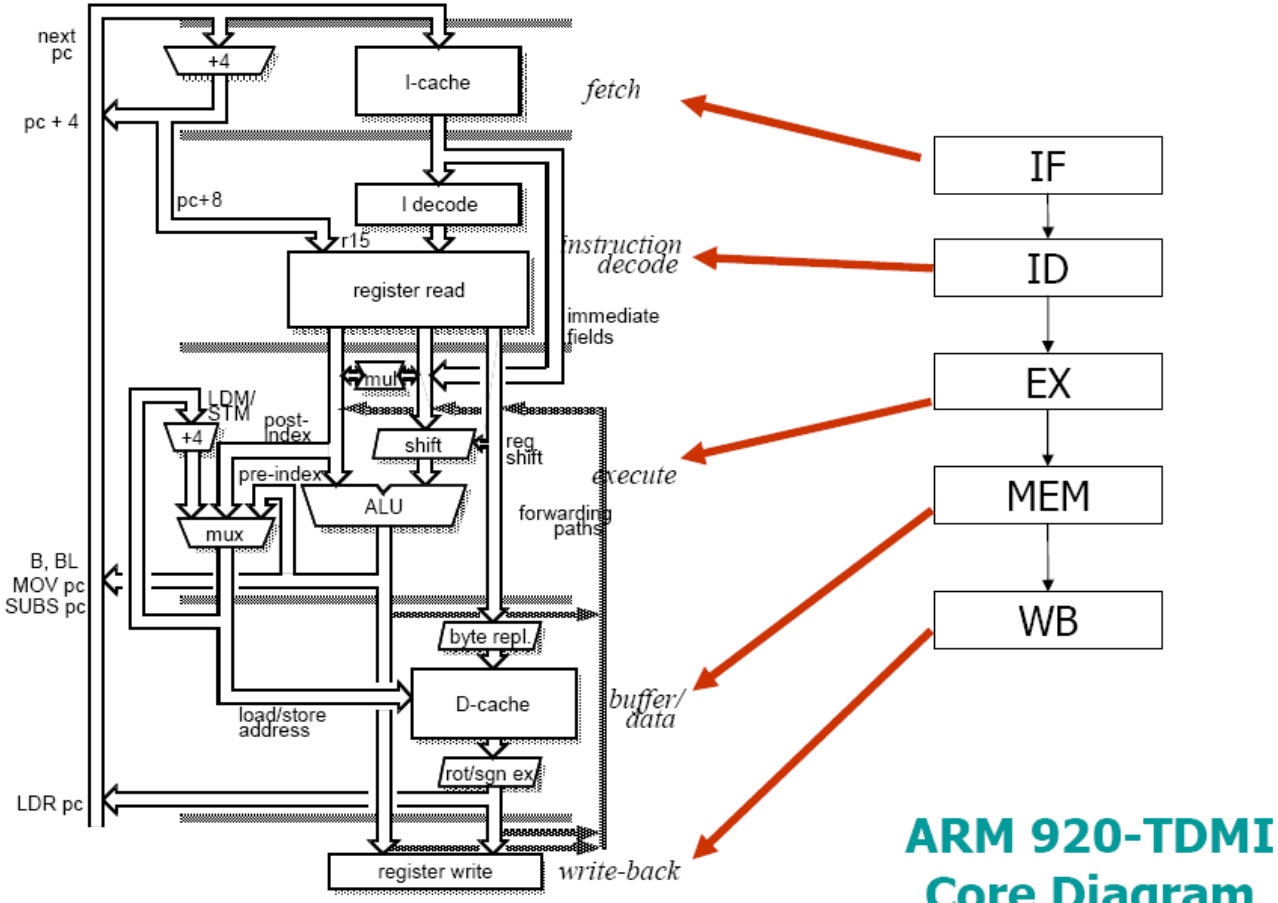


Figure 3 : The ARM9E-S core pipline



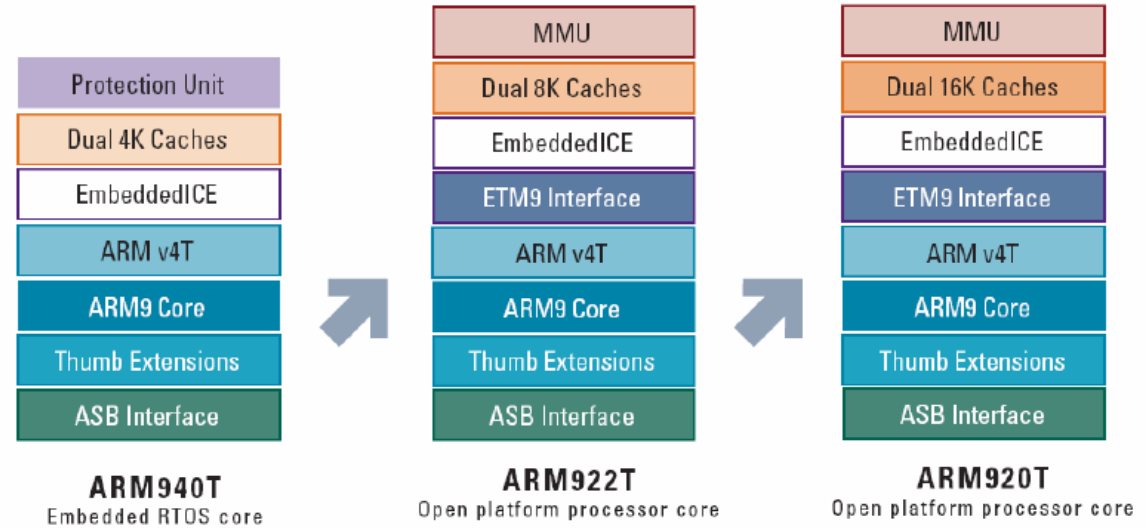
ARM 9 Processor Core



ARM 920-TDMI Core Diagram

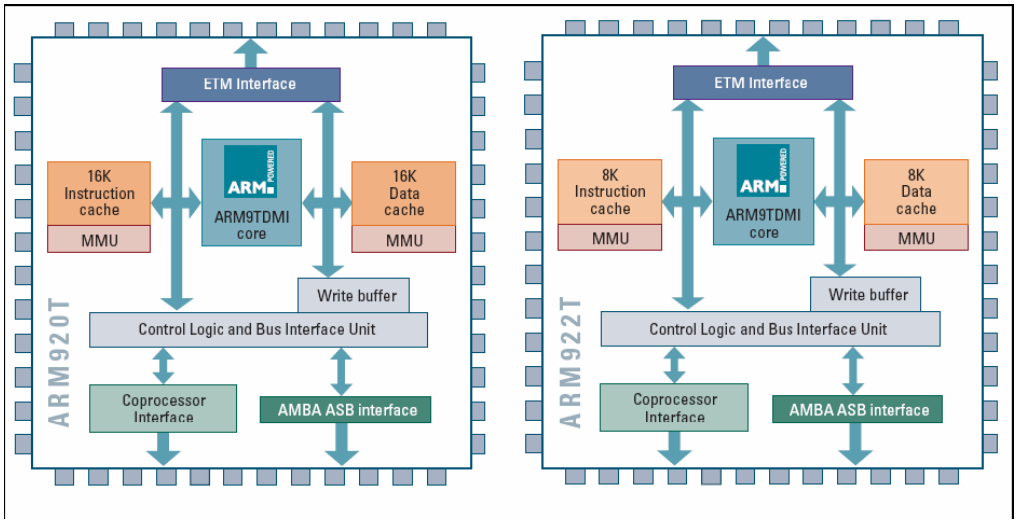
ARM 9 Processor Core

- Applications:
  - Next-generation hand-held products – Videophones, portable communicators, PDAs
  - Digital consumer products – Set-top boxes, home gateways, games consoles, MP3 audio, MPEG4 video
  - Imaging – Desktop printers, still picture cameras, digital video cameras
  - Automotive – Telematic and infotainment systems

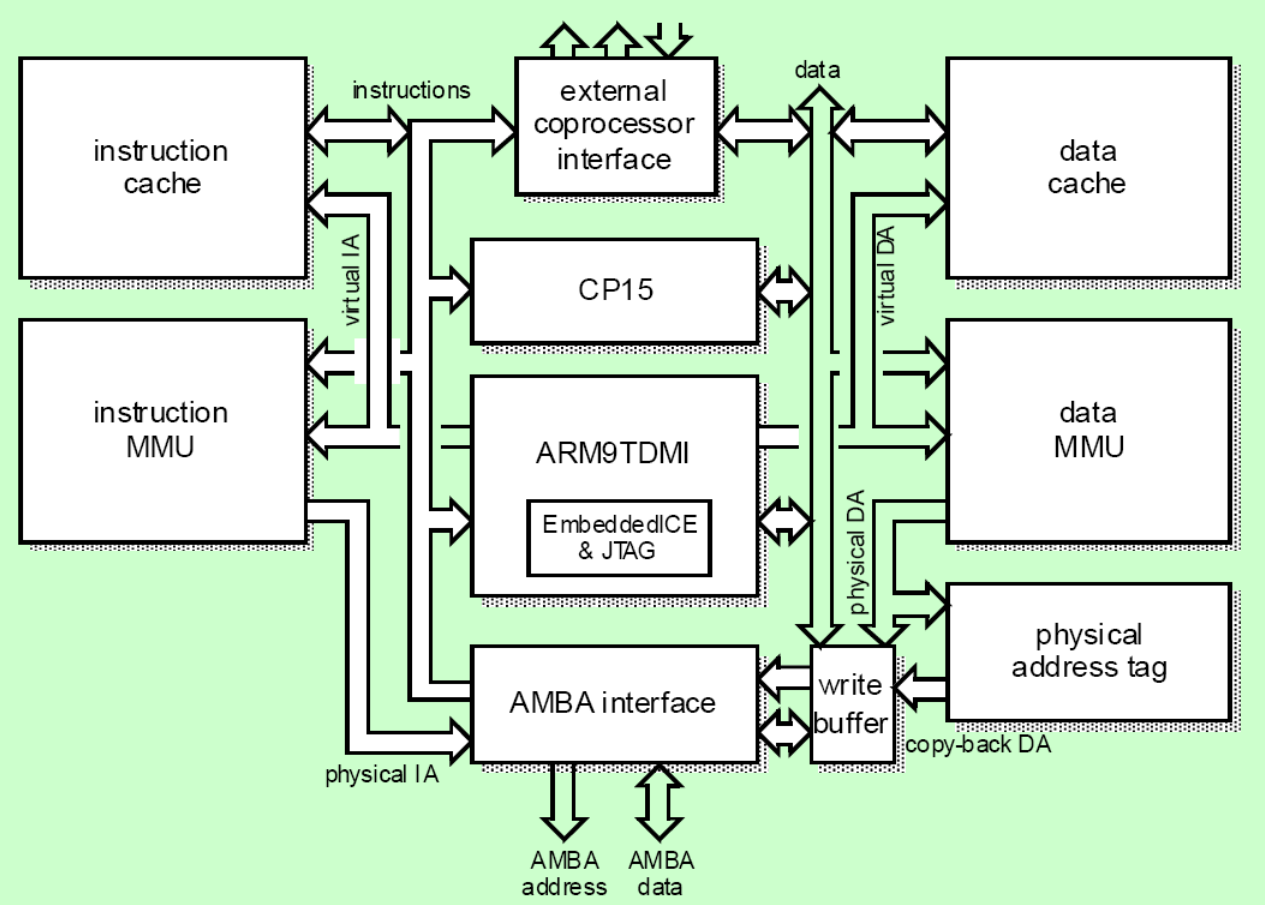


ARM920/922T Macrocells

- The ARM920T and ARM922T macrocells were designed to support platform operating systems such as Symbian OS, Linux, Windows CE and Palm OS
- well suited for hand-held, battery powered, wireless platforms like PDAs, 3G phones, smart phones and Internet appliances.
- The combination of the macrocell's high performance and cache lock-down features enable real-time functions such as video stream decoding and voicerecognition interfaces to be run on the same CPU as the operating system.

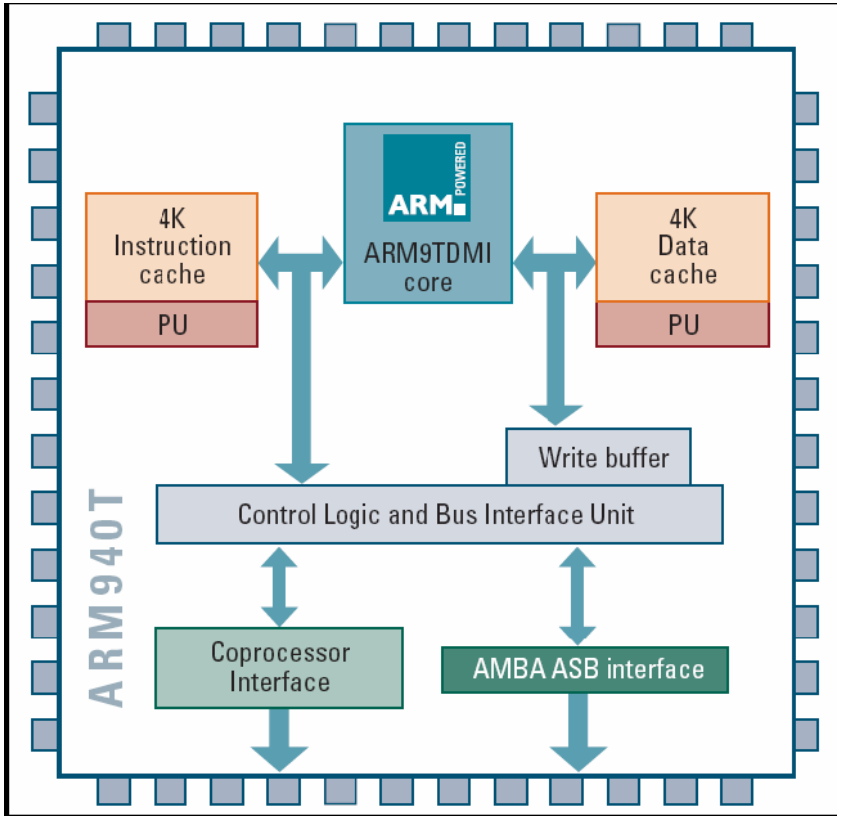


ARM920T organization

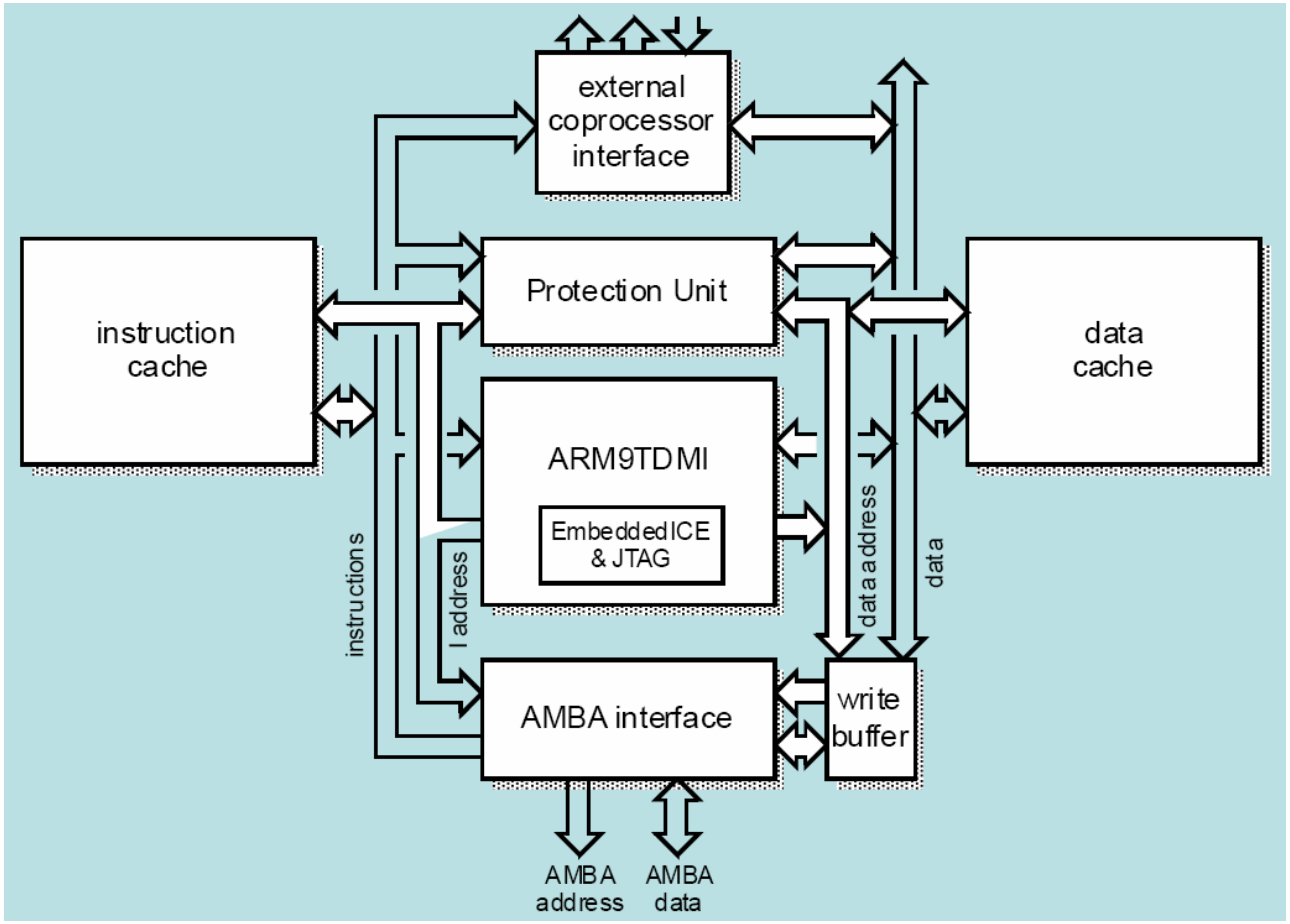


ARM940T Macrocell

- The ARM940T was designed for applications such as DSL and cable modem chipsets, network interface cards, printers and automotive control devices, where no additional system software is needed.
  - The ARM940T macrocell combines an ARM9TDMI processor core with 4k instruction cache and 4k data cache.
  - It also includes an MPU and an AMBA bus interface for SoC integration.
  - The protection unit allows definition of 8 regions of memory, each with independent cache, write buffer enable and access permissions.
  - The protection unit is configured via on-chip registers, providing a simple programmer's model and removing the need for pagemapping tables to be stored in memory.



ARM940T organization



ARM 9E

- The ARM9E family enable single core solutions for microcontroller, DSP and Java applications, offering savings in chip area and complexity, power consumption, and time-to-market.
- ARM9E Family Features
  - 32-bit RISC processor core with ARM®, Thumb® and DSP instruction sets
  - ARMJazelle technology delivers 8x Java acceleration (ARM926EJ-S)
  - 5-stage integer pipeline achieves 1.1 MIPS/MHz
  - Up to 300 MIPS (Dhrystone 2.1) in a typical 0.13µm process
  - Integrated real-time trace and debug support
  - Optional VFP9 coprocessor delivers floating-point performance
  - 215 MFLOPS for 3D graphics and real-time control systems
  - High-performance AHB system
  - MMU supporting Windows CE, Symbian OS, Linux, Palm OS (ARM926EJ-S)
  - Integrated instruction and data caches
  - Real-time debug support for SoC designers, including ETM interface
  - 16-entry write buffer — avoids stalling the processor when writes to external memory are performed
  - Flexible soft IP delivery, synthesizable to the latest 0.18µm, 0.15µm, 0.13µm silicon processes.

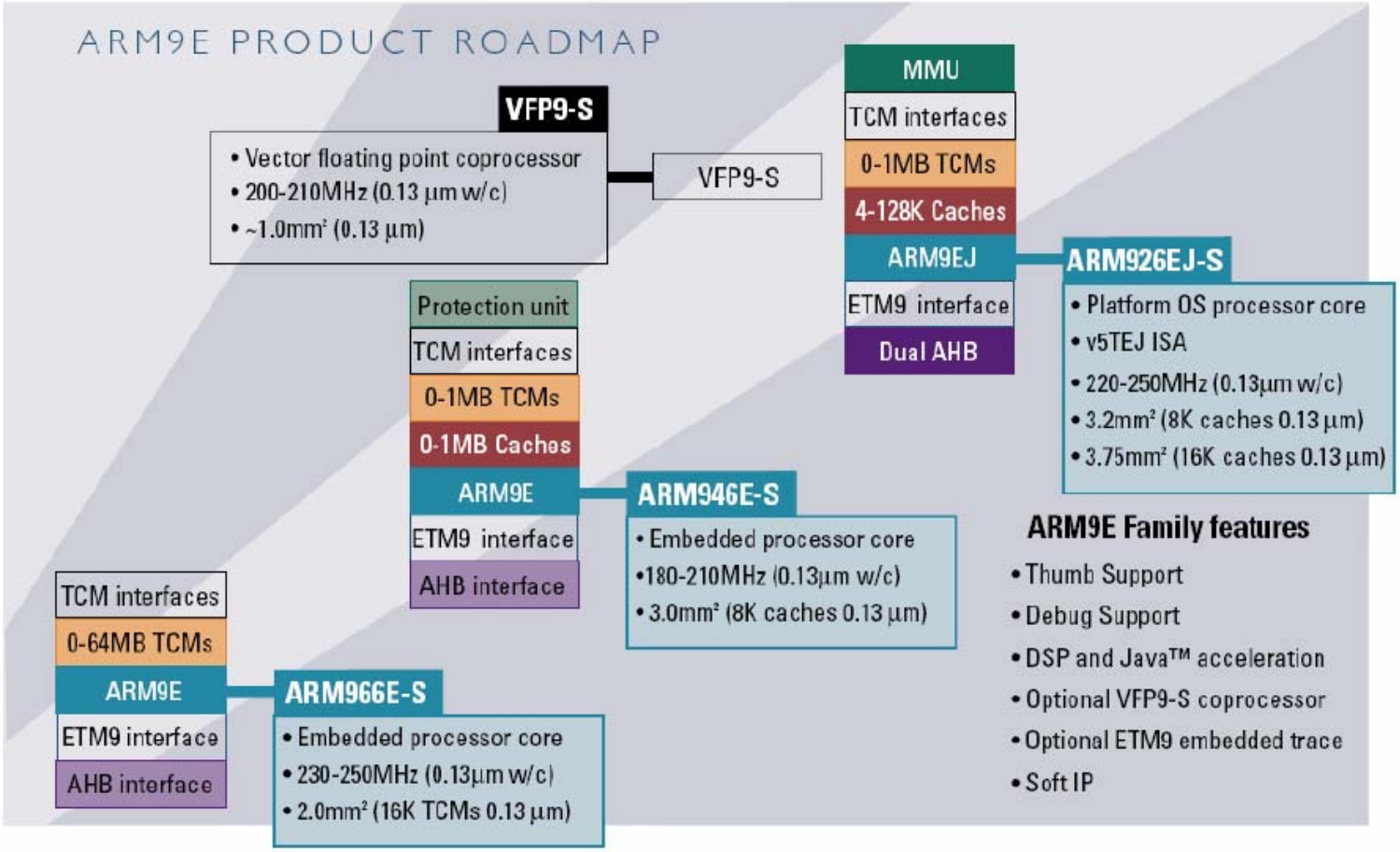
ARM 9E

- Applications:
  - Next-generation hand-held products – Videophones, portable communicators, Internet appliances
  - Digital consumer products – Set-top boxes, home gateways, games consoles,
  - Imaging – Desktop printers, still picture cameras, digital video cameras
  - Storage – HDD and DVD drives
  - Automotive – Powertrain, infotainment, ABS, body control systems
  - Industrial control systems – Motion controls, power delivery
  - Networking – VoIP, Wireless LAN, xDSL

PERFORMANCE CHARACTERISTICS

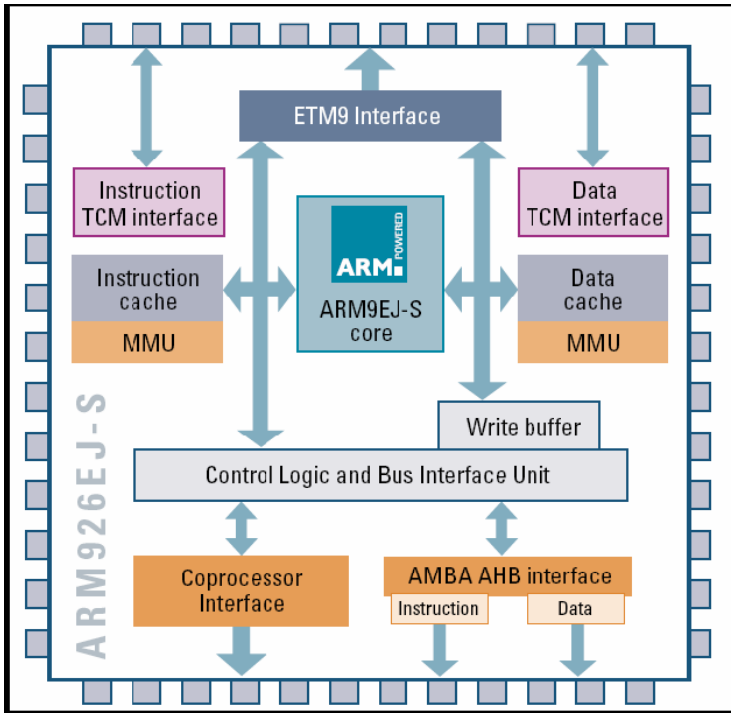
	Cache Size (Inst/Data)	Tightly Coupled Memory	Memory Mgt	Bus Interface	Thumb	DSP	Jazelle
ARM926EJ-S	Variable	Yes	MMU	2x AHB	Yes	Yes	Yes
ARM946E-S	Variable	Yes	MPU	AHB	Yes	Yes	No
ARM966E-S	-	Yes	-	AHB	Yes	Yes	No
ARM968E-S		Yes	DMA	AHB-Lite	Yes	Yes	No

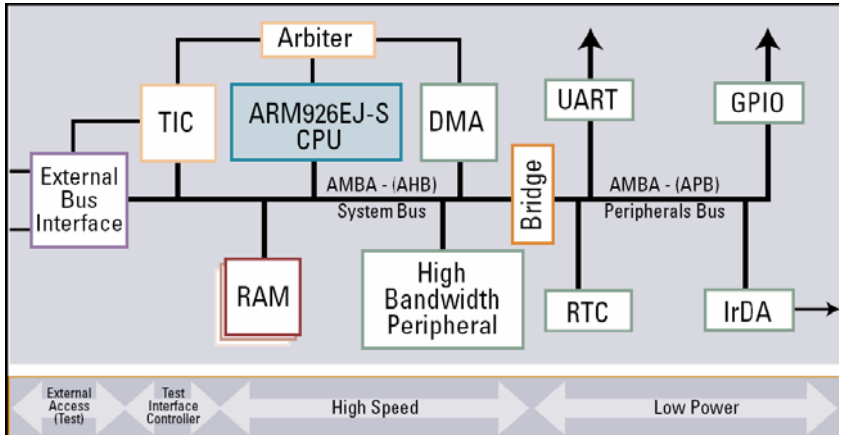
ARM 9E Products



ARM926EJ-S

- The ARM926EJ-S synthesizable macrocell combines a Jazelle™ technology enhanced CPU core with flexible size instruction and data cache, instruction and data tightly coupled memory (TCM) interfaces, memory management unit for applications running a Platform OS and instruction and data AMBA™ interconnect-based AHB interfaces.





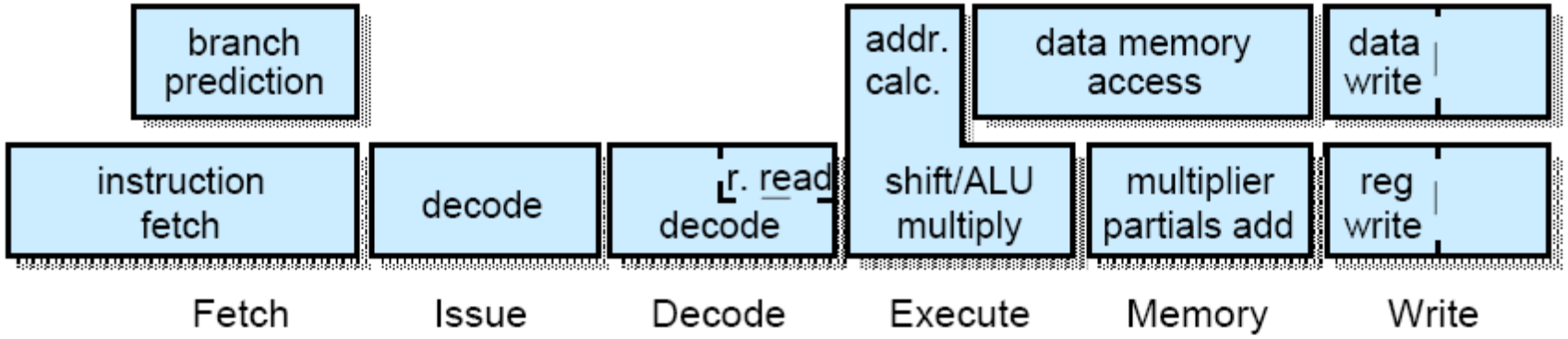
ARM 10E Family

- ARM 10E family offers an excellent combination of high performance and low power consumption, the ARM10E family includes new architectural features to deliver the highest MIPS/MHz of any ARM product. The family features new power-saving modes, 64-bit load-store micro-architecture, IEEE754 compatible floating-point coprocessor with vector operations, easy system integration, and a complete set of hardware and software development tools.
- ARM 10E Benefits
  - Modified Harvard Architecture
  - Can be ported to a wide range of processes and optimized for size and speed
  - ARM and Thumb instruction sets can be mixed to support application requirements for speed and code density
  - Fixed-point DSP instruction extensions reduce the need for separate and costly DSP processors
  - Small die size reduces overall SoC area, cost, and power consumption
  - Low power consumption enables cheaper packaging and cooling solutions, and increases reliability in the field
  - Instruction set can be extended for specific requirements using coprocessors
  - EmbeddedICE-RT and ETM10 units enable non-intrusive debug for hard real-time applications
  - Broad range of compatible application software, development tools and boards, services, and industry-leading OS

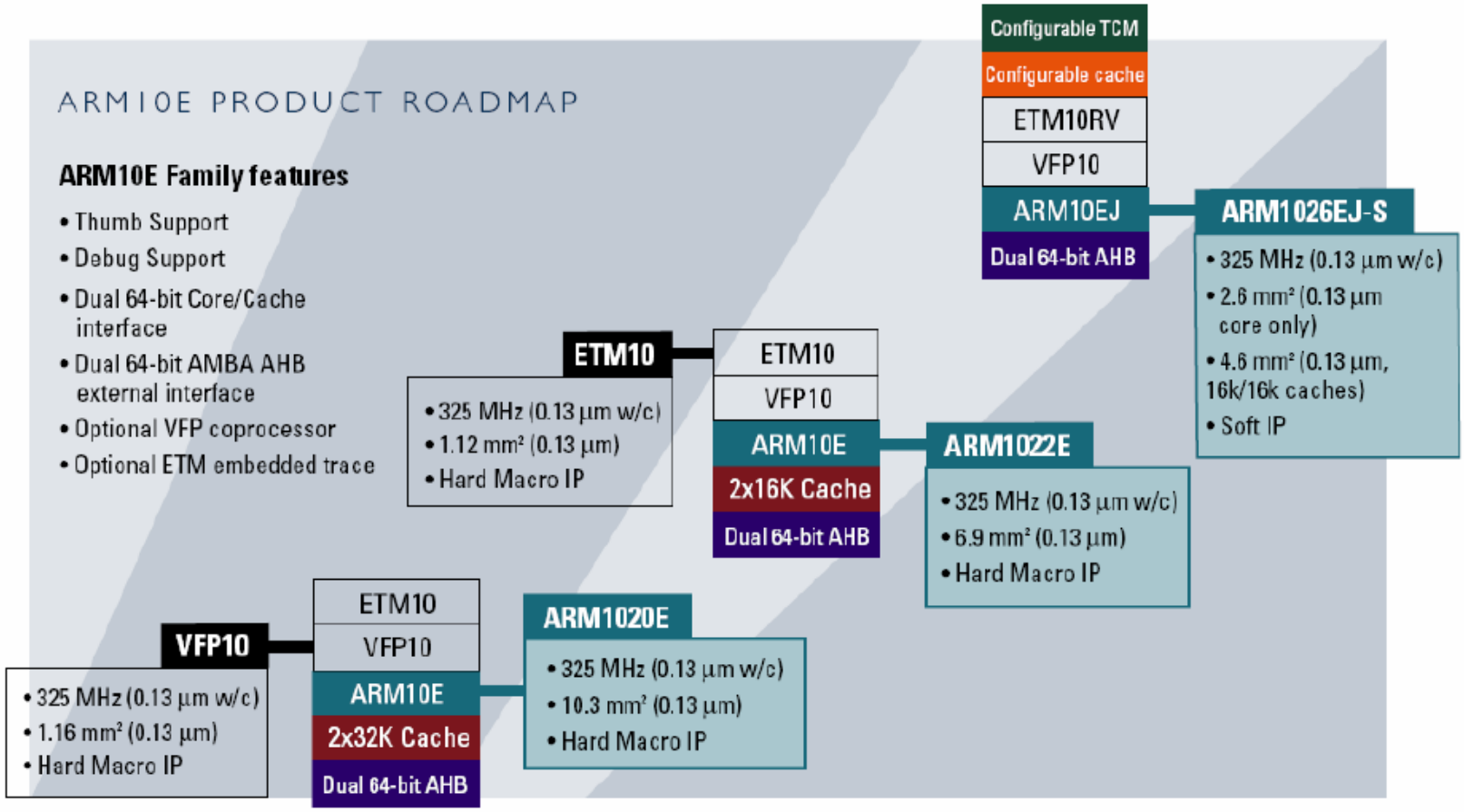
ARM10E Family

- Applications:
  - Next-generation hand-held products – Internet appliances, portable communicators and PDAs
  - Digital consumer products – Set-top boxes, home gateways, VoIP telephones, web tablets, laser printers, game consoles, digital cameras and TV
  - Automotive control systems – Powertrain control, drive-by-wire control, infotainment, navigation
  - Industrial control systems – Motion controls, power delivery, signal processing
- • Features:
  - 32/16-bit RISC architecture (ARMv5TE)
  - 32-bit ARM instruction set for maximum performance and flexibility
  - 16-bit Thumb instruction set for increased code density
  - DSP instruction extensions and single cycle MAC
  - Instruction and data caches: ARM1020E = 32K/32K, ARM1022E 16K/16K
  - Individual lockable cache/MMU entries
  - ARM and Thumb instruction sets, including fixed-point DSP extensions
  - 64-bit high-bandwidth internal bus architecture with multiple execution units
  - Advanced energy saving power-down modes to address static leakage currents
  - Dual 64-bit AMBA bus-compliant AHB interfaces
  - Optional VFP10 vector floating point coprocessor
  - Optional ETM10 embedded trace macrocell for non-intrusive real-time debug

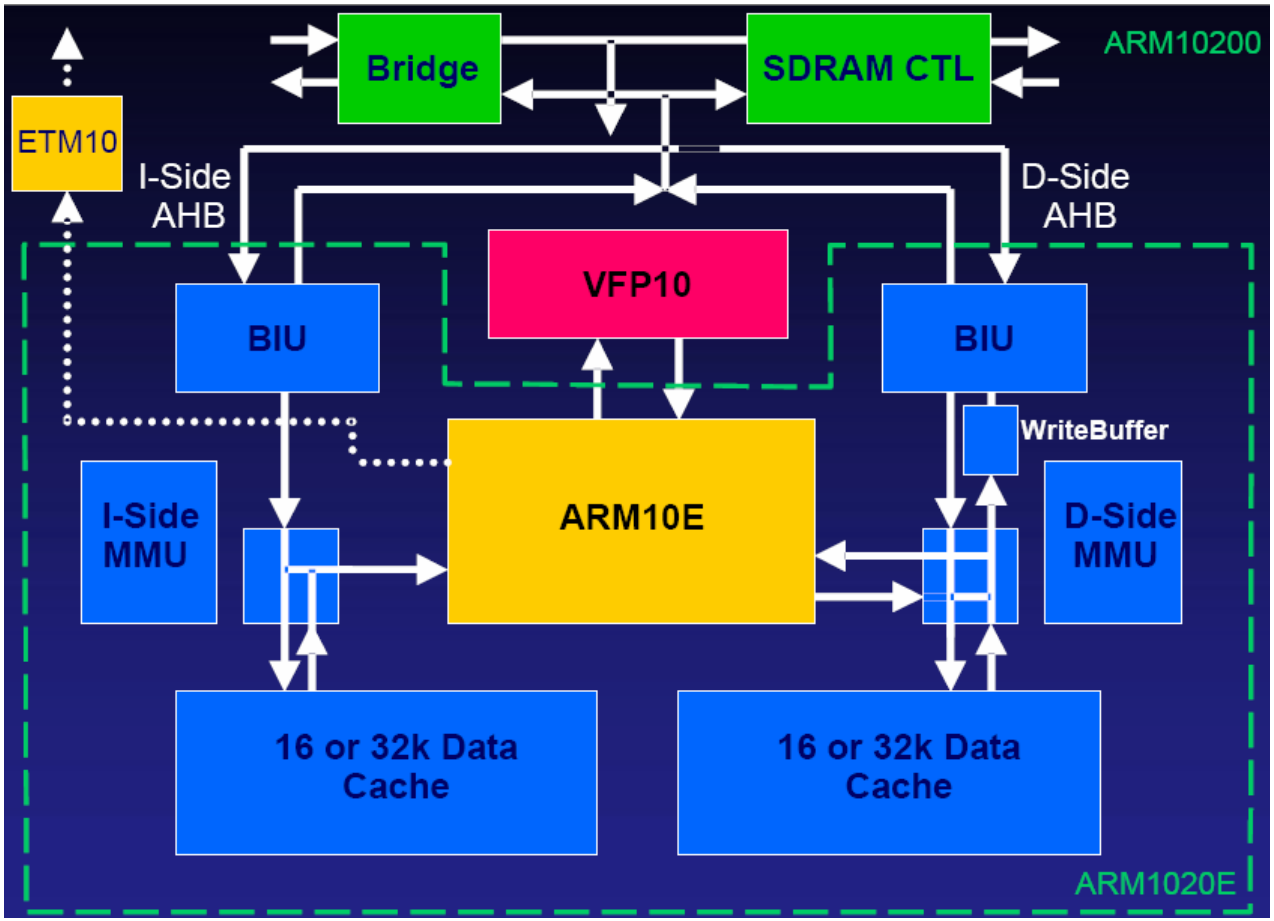
The ARM10TDMI pipeline



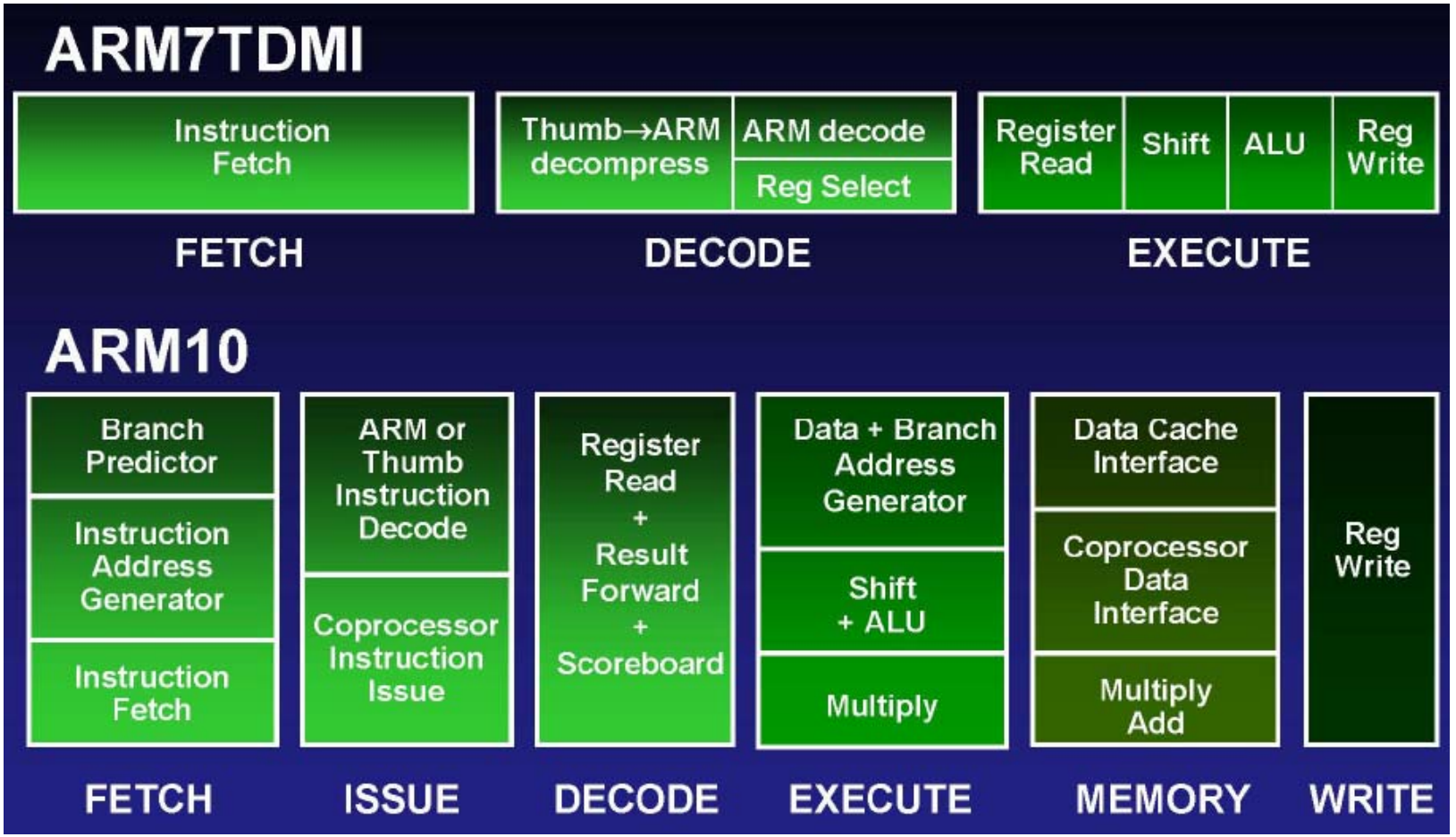
ARM10E Family



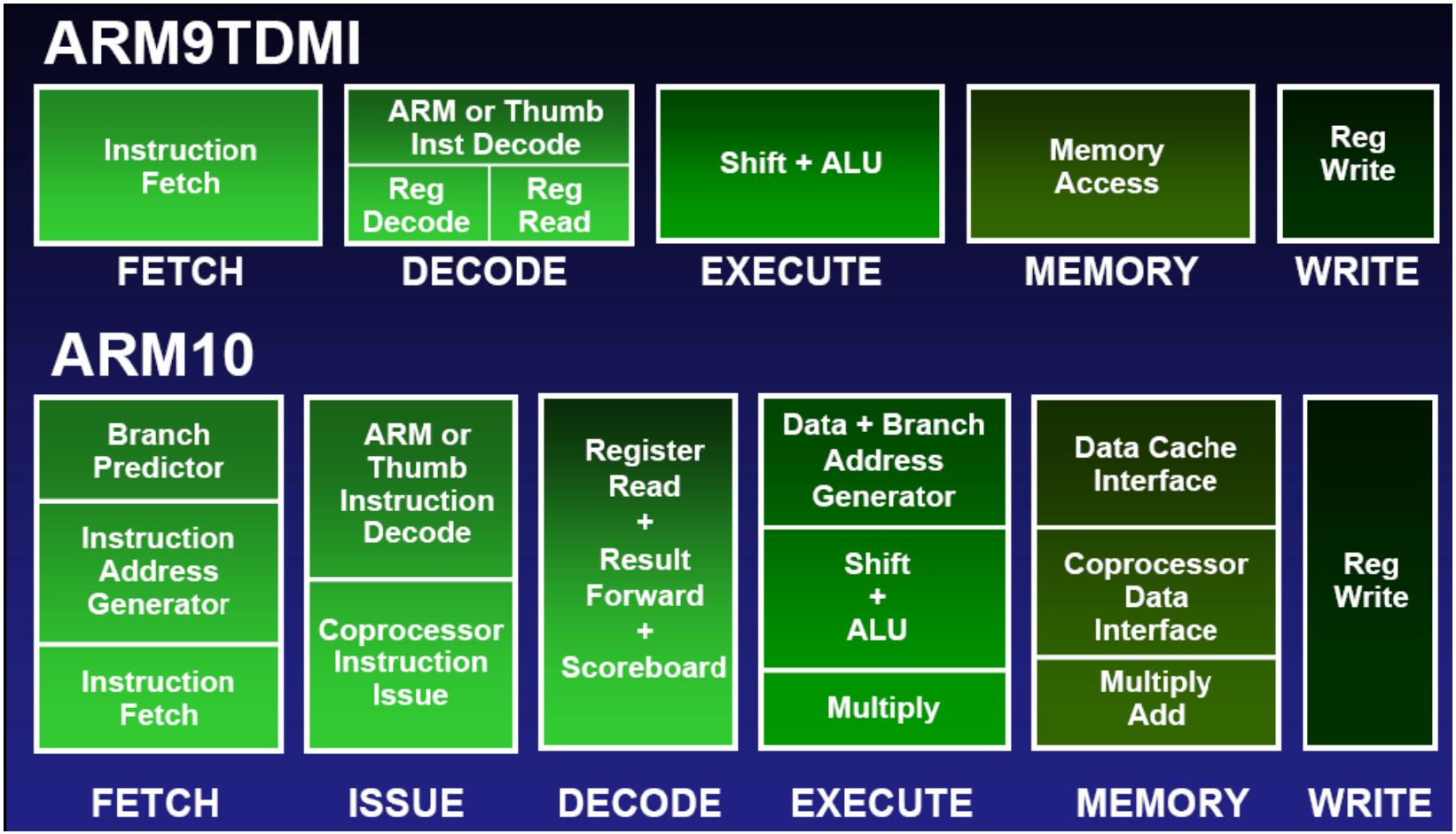
ARM1020E Core



Comparison of ARM7 and ARM10 Pipelines

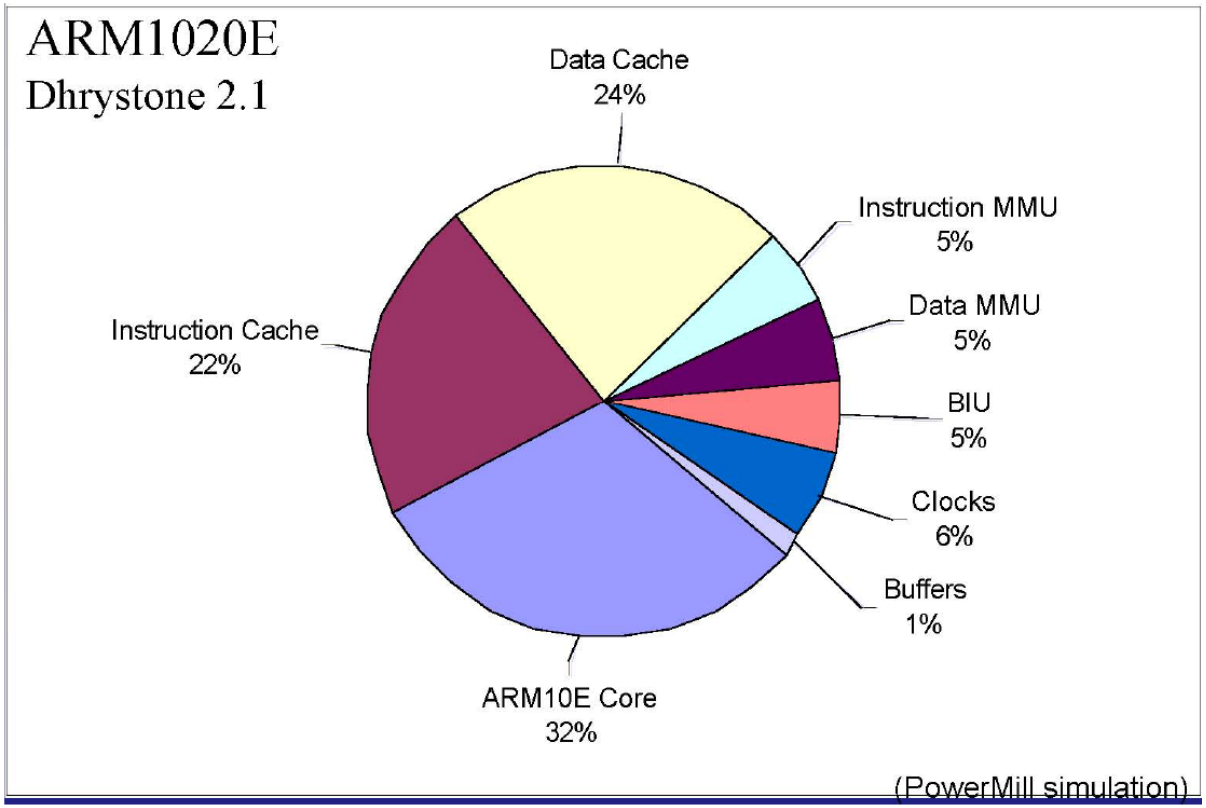


Comparison of ARM9 and ARM10 Pipelines



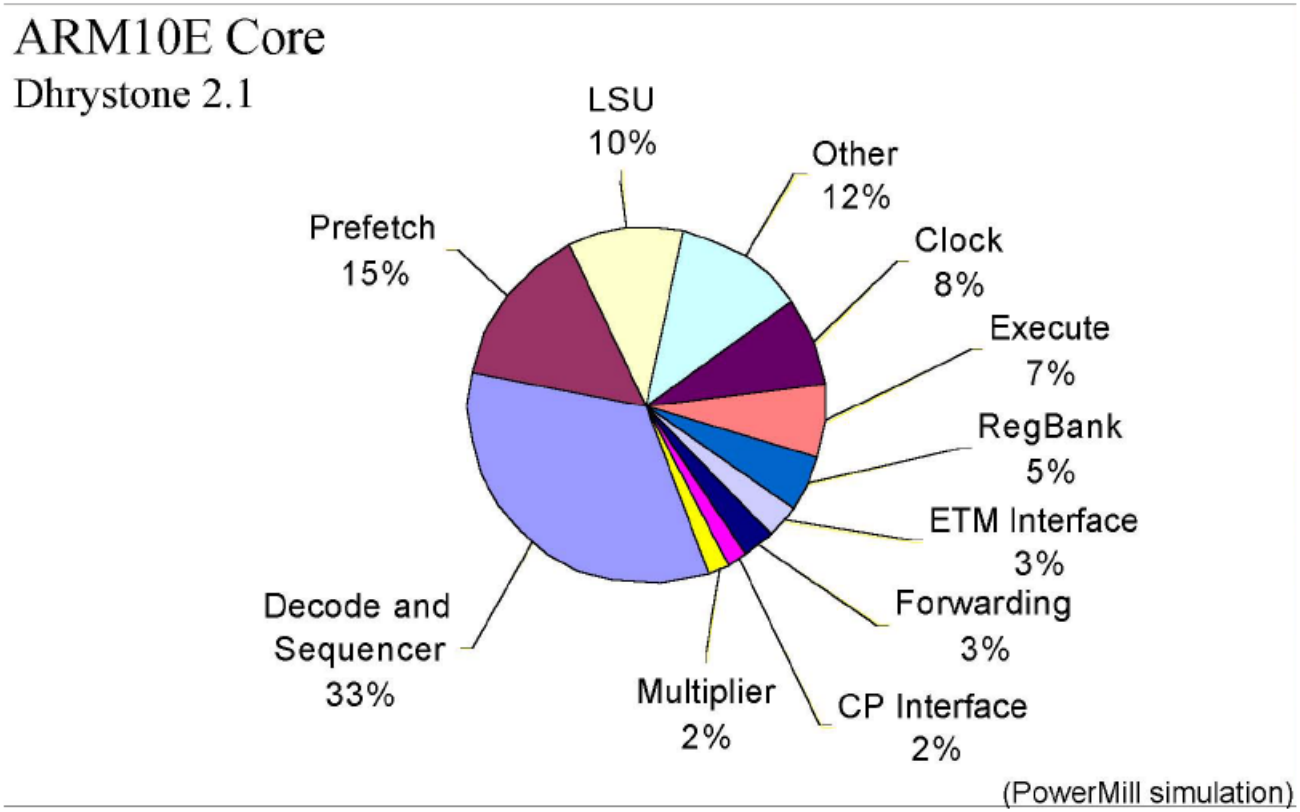
Power Consumption Chart

- Consumption in various Functional Units



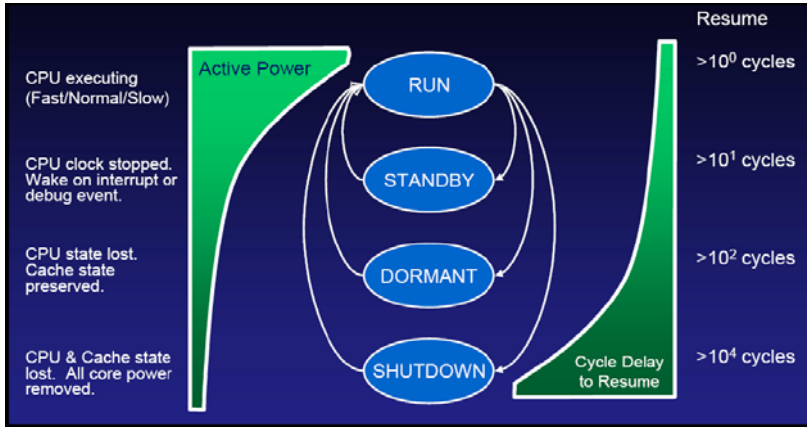
Power Consumption Chart

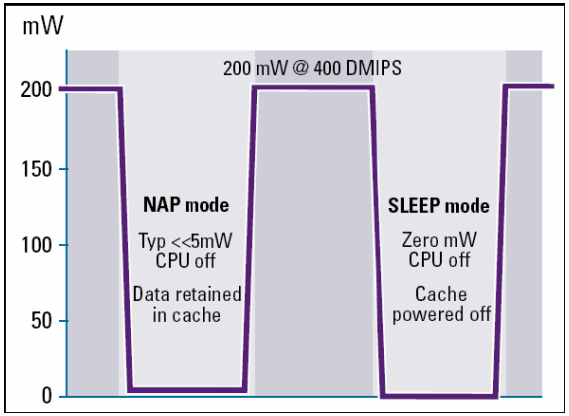
Consumption in various Operational Units



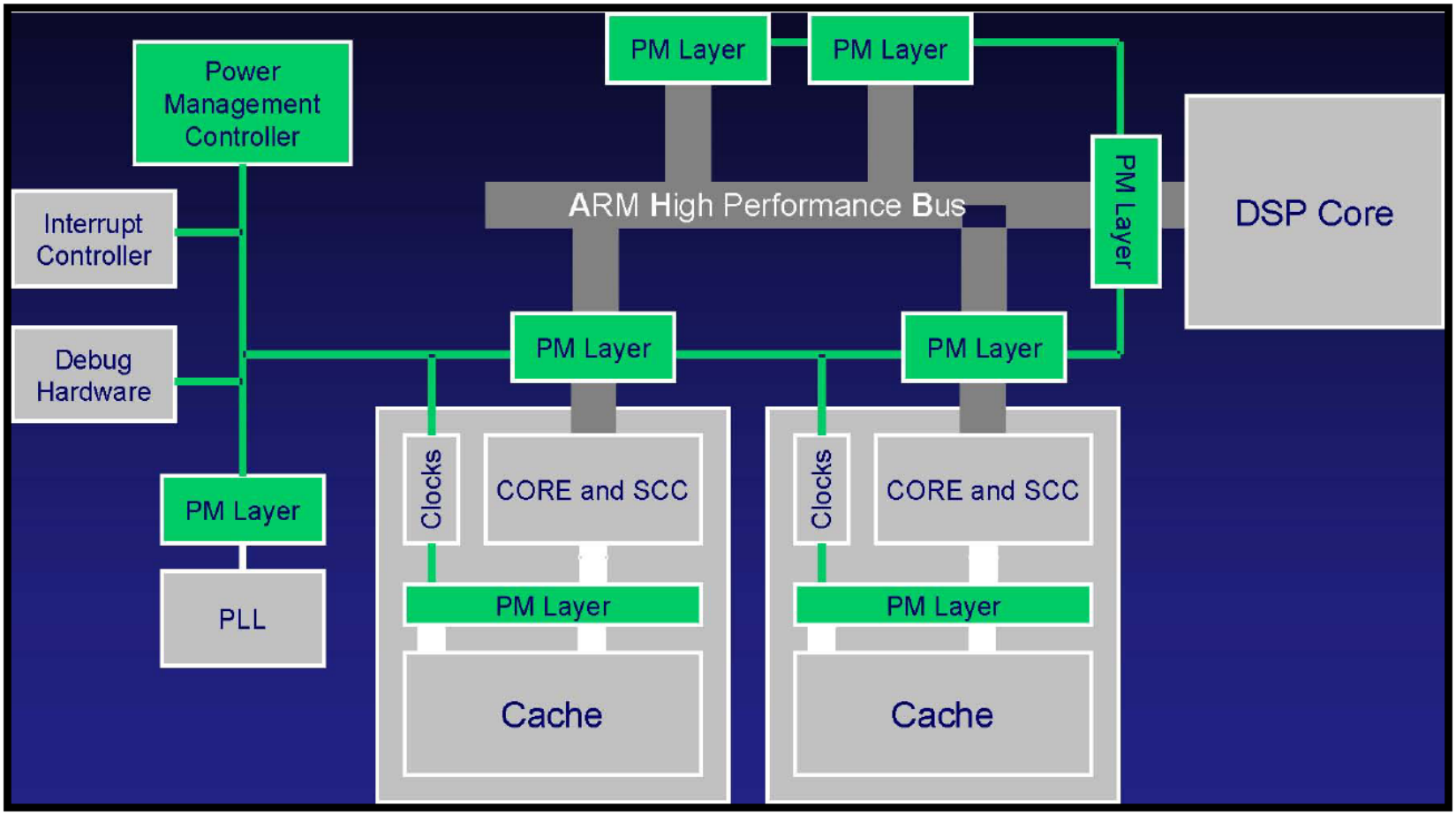
Power Efficiency in ARM10

- The ARM10 family's exceptional power/performance ratings and advanced power-down modes help to ensure that system designs meet the most demanding customer expectations:
- NAP: power-down core (preserves state in caches) << 5 Mw standby power.
- SLEEP: power-down entire ARM1020E (state must be stored in memory). Zero power with fast wake-up.

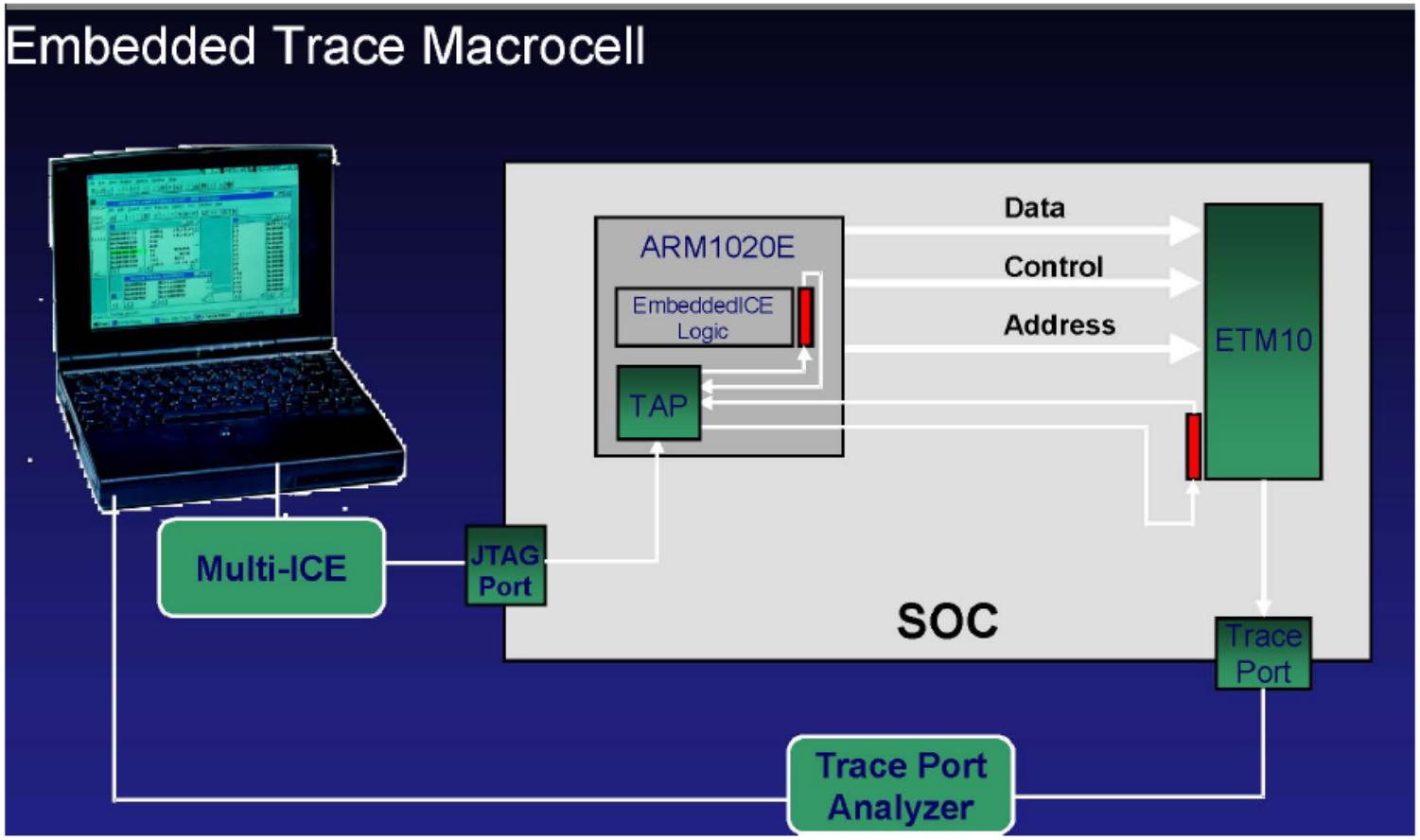




Processor Snap in Power Down Mode



ARM10 ETM10 Cell



ETM10

- Full real-time instruction and data tracing
  - Monitors the core's *internal* buses
- Zero performance overhead
- Supports high frequency trace with demux-port
- Configurable synthesis for optimum:
  - area
  - features
  - pin count
- Programmed non-intrusively through JTAG

ARM1020E Die

ARM1020E:

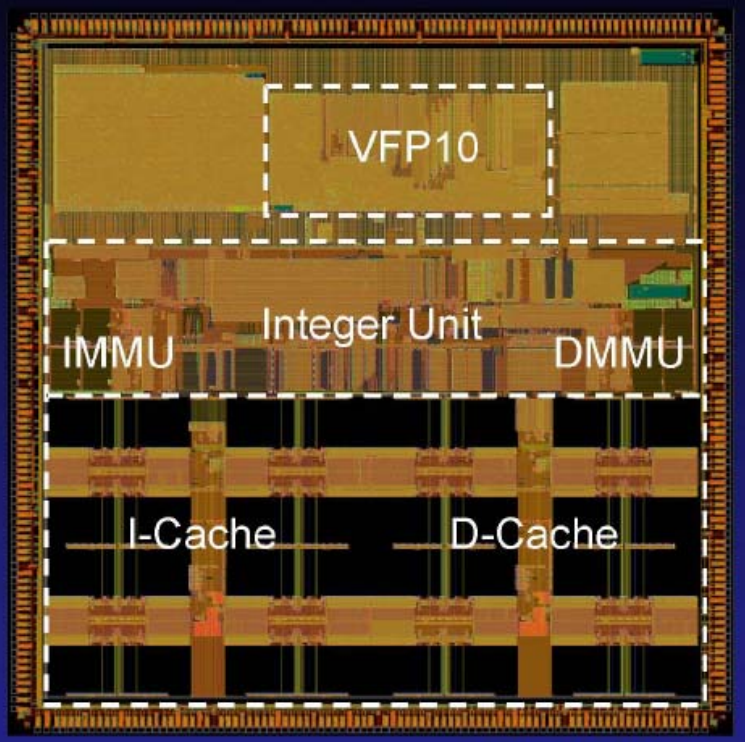
- 500 DMIPS @400 MHz
- 0.51 mA/MIPS
- 10.3mm^2 / 6.9mm^2

VFP10:

- 236 MFLOPS @400MHz
- IEEE 754 Compatible

ETM10:

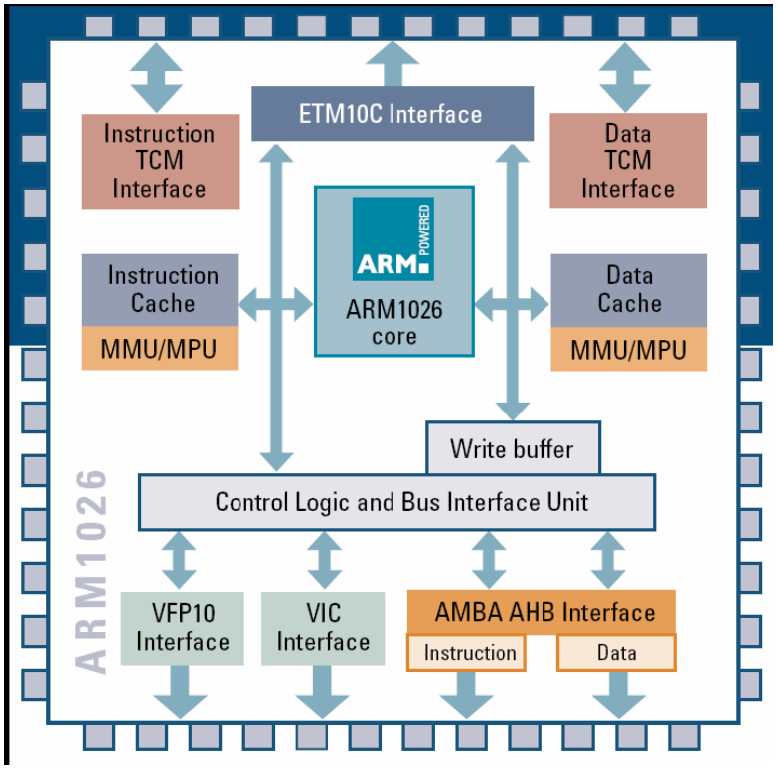
- Full speed, real time embedded trace



(ARM10200r1)

ARM1026J-S Core

- ARM1026EJ-S is a fully synthesizable processor featuring
  - a Jazelle technology enhanced CPU,
  - memory management and protection units,
  - DSP instruction set extensions,
  - configurable caches and TCMs,
  - dual 64-bit AMBA AHB interfaces,
  - optional vector floating point coprocessor and
  - Embedded Trace Macrocell, ETM10RV.



ARM11 Family

- Based on the ARM11 microarchitecture, the ARM11 core family comprises a range of high performance microprocessor cores, delivering up to 740 Dhrystone 2.1 MIPS in 0.13μ process technology. The family comprises three main product lines optimized for the specific requirements of different market segments, each of which is available with an optional floating point coprocessor.

	ARM1136J(F)-S	ARM1156T2(F)-S	ARM1176JZ(F)-S
Automotive	Infotainment, DVD, navigation	Power train, body	*
Computer	PDA	Printer, data storage	PDA
Consumer	Digital TV, DVD, PVR, Set-top box, games	Digital camera	Set-top box*
Industrial	-	Embedded control	EPOS terminal
Networking	Infrastructure, switch/router	Modem	*
Wireless	Smartphone , applications processor	Base station	Combined applications and base-band processor for Smartphone

ARM11 Family Features

- Powerful ARMv6 instruction set architecture
- ARM Thumb instruction set reduces memory bandwidth and size requirements by up to 35%
- ARM Jazelle technology for efficient embedded Java execution
- ARM DSP extensions
- SIMD (Single Instruction Multiple Data) media processing extensions deliver up to 2x performance for video processing
- ARM TrustZone technology for on-chip security foundation (ARM1176JZ-S and ARM1176JZF-S cores)
- Thumb-2 core technology for enhanced performance, energy efficiency and code density (ARM1156T2-S and ARM1156T2F-S cores)
- Low power consumption:
- 0.6mW/MHz (0.13µm, 1.2V) including cache controllers
- Energy saving power-down modes address static leakage currents in advanced processes
- Intelligent Energy Manager (IEM) technology for dynamic power management (ARM1176JZ-S and ARM1176JZF-S cores)
- High performance integer processor
- 8-stage integer pipeline delivers high clock frequency (9 stages for ARM1156T2(F)-S)
- Separate load-store and arithmetic pipelines
- Branch Prediction and Return Stack
- High performance memory system design
- Supports 4-64k cache sizes
- Optional tightly coupled memories with DMA for multi-media applications
- High-performance 64-bit memory system speeds data access for media processing and networking applications
- ARMv6 memory system architecture accelerates OS context-switch
- Vectored interrupt interface and low-interrupt-latency mode speeds interrupt response and real-time performance
- Optional Vector Floating Point coprocessor (ARM1136JF-S, ARM1176JZF-S and ARM1156T2F-S cores) for automotive/industrial controls and 3D graphics acceleration
- All ARM11 cores are delivered as ARM- Synopsys Reference Methodology compliant deliverables which significantly reduce the time to generate a specific technology implementation of the core and to generate a complete set of industry standard views and models.

ARM11Pipeline

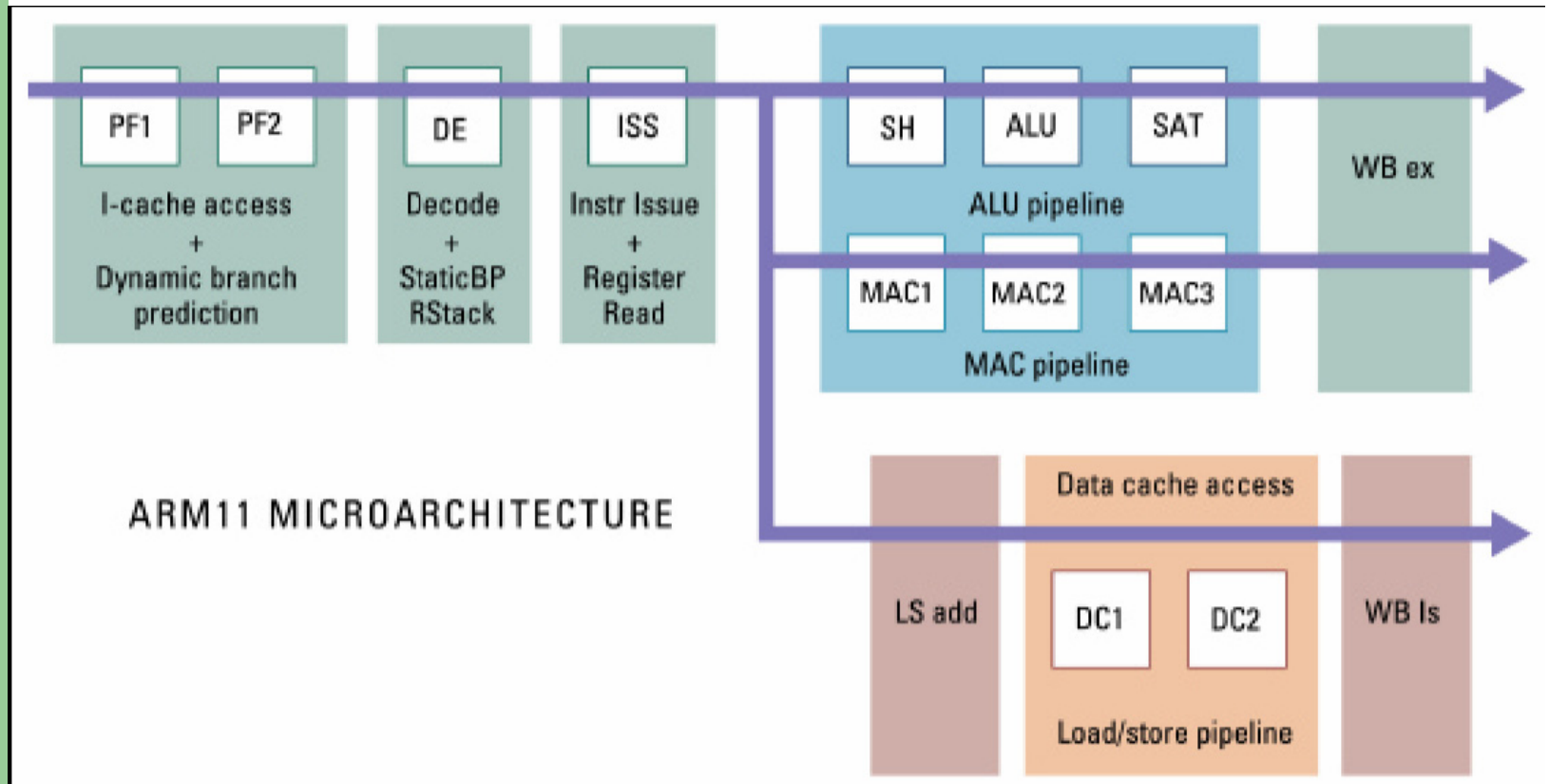


Figure 3. ARM11 Pipeline Structure

ARM Family Comparison

Feature	ARM9E™	ARM10E™	Intel® XScale™	ARM11™
Architecture **Pipeline Length**	ARMv5TE(J) 5	ARMv5TE(J) 6	ARMv5TE 7	ARMv6 8
Java Decode	(ARM926EJ)	(ARM1026EJ)	No	Yes
V6 SIMD Instructions	No	No	No	Yes
MIA Instructions	No	No	Yes	Available as coprocessor
Branch Prediction	No	Static	Dynamic	Dynamic
Independent Load-Store Unit	No	Yes	Yes	Yes
Instruction Issue	Scalar, in-order	Scalar, in-order	Scalar, in-order	Scalar, in-order
Concurrency	None	ALU/MAC, LSU	ALU, MAC, LSU	ALU/MAC, LSU
Out-of-order completion	No	Yes	Yes	Yes
Target Implementation	Synthesizable	Synthesizable	Custom chip	Synthesizable and Hard macro
Performance Range	Up to 250MHz	Up to 325MHz	200MHz – >1GHz	350MHz - >1GHz

References

- 1. http://www.arm.com/
- 2. ARM System-on-Chip Architecture by S. Furber; *Chapters 9 & 12*. Addison Wesley Longman: ISBN 0-201-67519-6
- 3.http://www.arm.com/products/CPUs/architecture.html
- 4.http://www.cs.umd.edu/class/fall2001/cmsc411/proj01/arm/armch ip.html
- 5.http://www.arm.com/products/solutions/AMBAHomePage.html