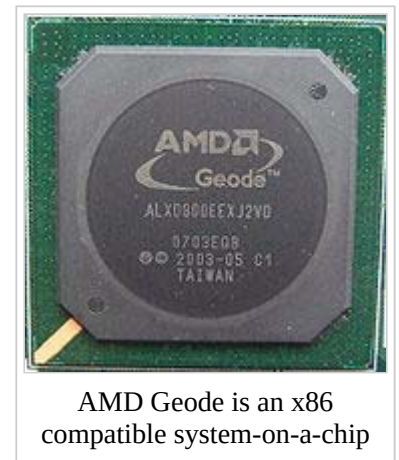


System-on-a-chip

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(Redirected from System on chip)

System-on-a-chip or **system on chip** (**SoC** or **SOC**) refers to integrating all components of a computer or other electronic system into a single integrated circuit (chip). It may contain digital, analog, mixed-signal, and often radio-frequency functions – all on one. A typical application is in the area of embedded systems.

The contrast with a microcontroller is one of degree. Microcontrollers typically have under 100K of RAM (often just a few KBytes) and often really *are* single-chip-systems; whereas the term SoC is typically used with more powerful processors, capable of running software such as Windows or Linux, which need external memory chips (flash, RAM) to be useful, and which are used with various external peripherals. In short, for larger systems *System-on-a-chip* is hyperbole, indicating technical direction more than reality: increasing chip integration to reduce manufacturing costs and to enable smaller systems. Many interesting systems are too complex to fit on just one chip built with a process optimized for just one of the system's tasks.



AMD Geode is an x86 compatible system-on-a-chip

When it is not feasible to construct an SoC for a particular application, an alternative is a system in package (SiP) comprising a number of chips in a single package. In large volumes, SoC is believed to be more cost effective than SiP since it increases the yield of the fabrication and because its packaging is simpler.^[1]

Another option, as seen for example in higher end cell phones and on the Beagleboard, is package on package stacking during board assembly. The SoC chip includes processors and numerous digital peripherals, and comes in a ball grid package with lower and upper connections. The lower balls connect to the board and various peripherals, with the upper balls in a ring holding the memory busses used to access NAND flash and DDR2 RAM. Memory packages could come from multiple vendors.

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Structure

A typical SoC consists of:

- One microcontroller, microprocessor or DSP core(s). Some SoCs – called multiprocessor System-on-Chip (MPSoC) – include more than one processor core.
- Memory blocks including a selection of ROM, RAM, EEPROM and Flash.
- Timing sources including oscillators and phase-locked loops.
- Peripherals including counter-timers, real-time timers and power-on reset generators.
- External interfaces including industry standards such as USB, FireWire, Ethernet, USART, SPI.
- Analog interfaces including ADCs and DACs.

- Voltage regulators and power management circuits.

These blocks are connected by either a proprietary or industry-standard bus such as the AMBA bus from ARM. DMA controllers route data directly between external interfaces and memory, by-passing the processor core and thereby increasing the data throughput of the SoC.

Design flow

An SoC consists of both the hardware described above, and the software that controls the microcontroller, microprocessor or DSP cores, peripherals and interfaces. The design flow for an SoC aims to develop this hardware and software in parallel.

Most SoCs are developed from pre-qualified hardware blocks for the hardware elements described above, together with the software drivers that control their operation. Of particular importance are the protocol stacks that drive industry-standard interfaces like USB. The hardware blocks are put together using CAD tools; the software modules are integrated using a software development environment.

A key step in the design flow is emulation: the hardware is mapped onto an emulation platform based on a field programmable gate array (FPGA) that mimics the behavior of the SoC, and the software modules are loaded into the memory of the emulation platform. Once programmed, the emulation platform enables the hardware and software of the SoC to be tested and debugged at close to its full operational speed. (Emulation is generally preceded by extensive software simulation. In fact, sometimes the FPGAs are used primarily to speed up some parts of the simulation work.)

After emulation the hardware of the SoC follows the place and route phase of the design of an integrated circuit before it is fabricated.

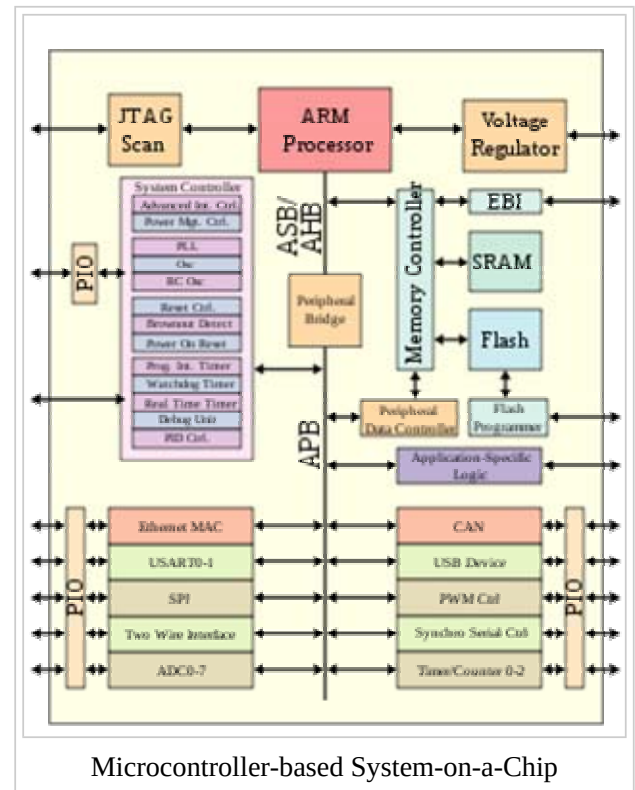
Chips are verified for logical correctness before being sent to foundry. This process is called functional verification, and it accounts for a significant portion of the time and energy expended in the chip design life cycle (although the often quoted figure of 70% is probably an exaggeration).^[2] Verilog and VHDL are typical hardware description languages used for verification. With the growing complexity of chips, hardware verification languages like SystemVerilog, SystemC, e, and OpenVera are also being used. Bugs found in the verification stage are reported to the designer.

Fabrication

SoCs can be fabricated by several technologies, including:

- Full custom
- Standard cell
- FPGA

SoC designs usually consume less power and have a lower cost and higher reliability than the multi-chip systems that they replace. And with fewer packages in the system, assembly costs are reduced as well.



However, like most VLSI designs, the total cost is higher for one large chip than for the same functionality distributed over several smaller chips, because of lower yields and higher NRE costs.

See also

- List of system-on-a-chip suppliers
- PSoC
- ASIC
- Microcontroller
- Electronic design automation
- Post silicon validation
- System in package
- Network On Chip

Notes

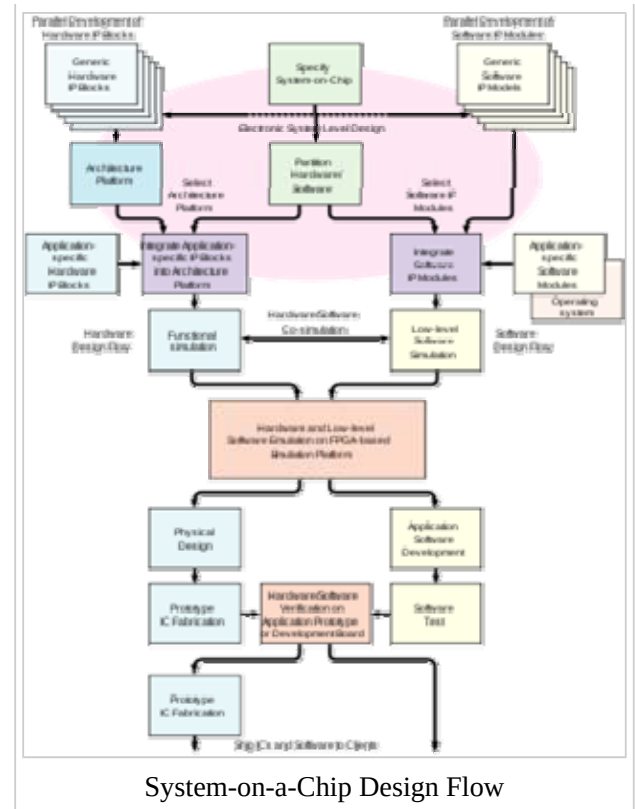
1. ^ "The Great Debate: SOC vs. SIP". Eetimes.com. <http://www.eetimes.com/showArticle.jhtml?articleID=159901628>. Retrieved 2009-08-12.
2. ^ "Is verification really 70 percent?". Eetimes.com. <http://www.eetimes.com/showArticle.jhtml?articleID=21700028>. Retrieved 2009-08-12.

External links

- SOCC Annual IEEE International SOC Conference

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