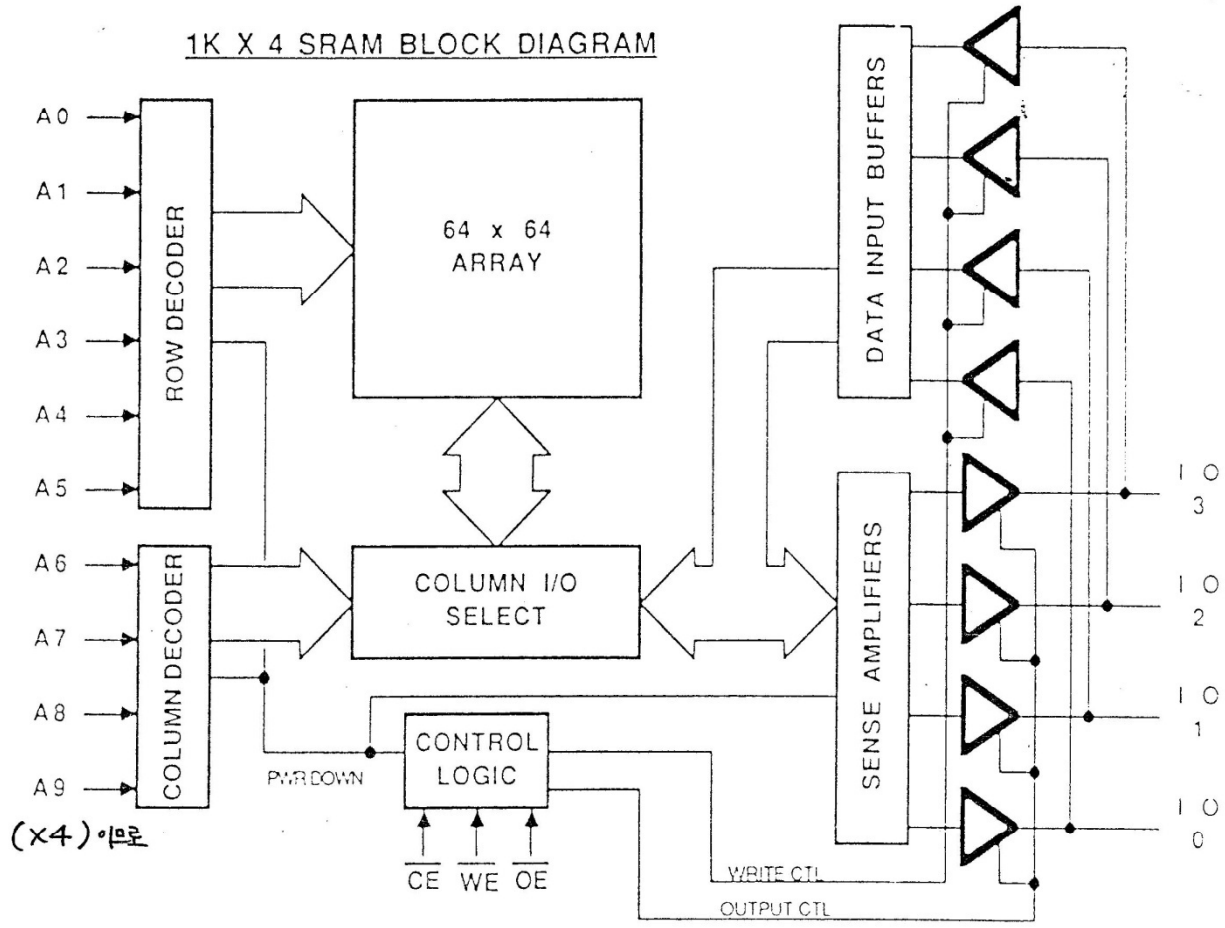
Static Random Access Memories (sRAM)

Instructor - Bruce Bateman, Cypress Semiconductor

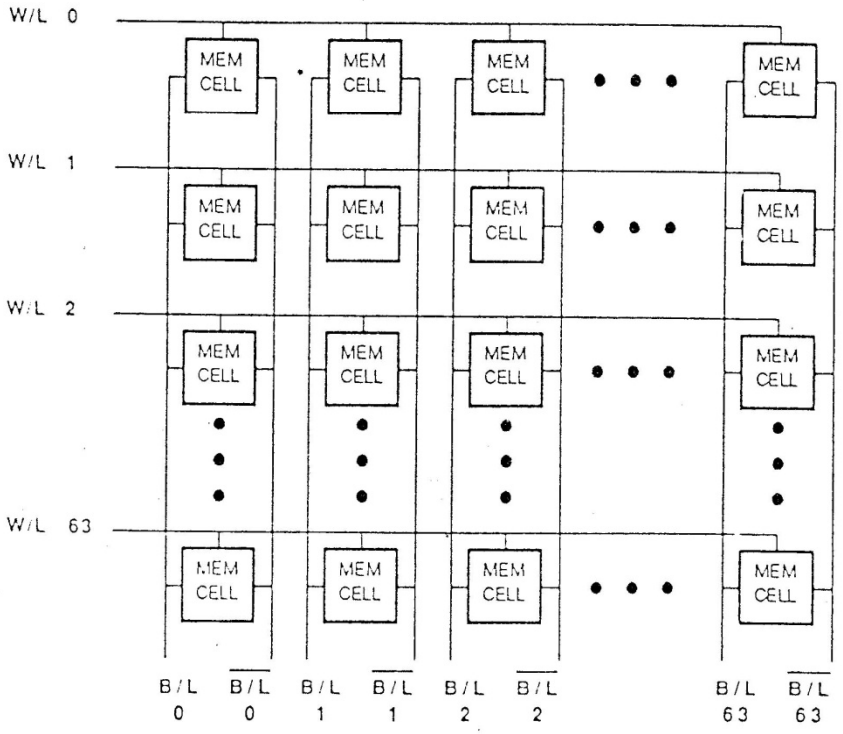
- Basic Architecture
- Storage Cell
- Address Decoding
- Data Sensing
- READ/WRITE Control

1K X 4 SRAM BLOCK DIAGRAM

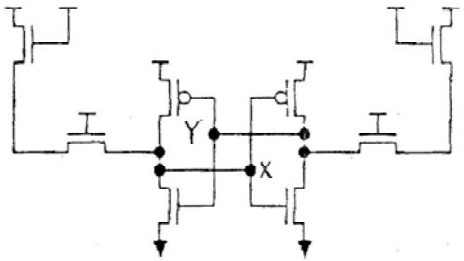


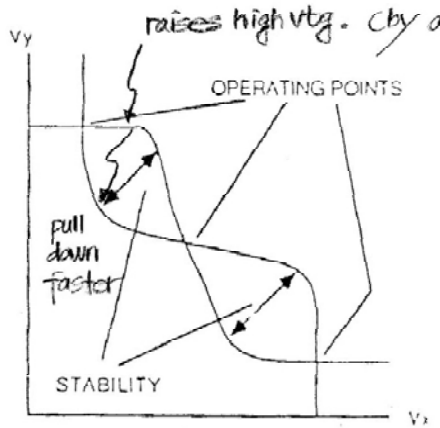
(x4)이므로

4K SRAM MEMORY ARRAY



6T MEMORY CELL "READ" STABILITY



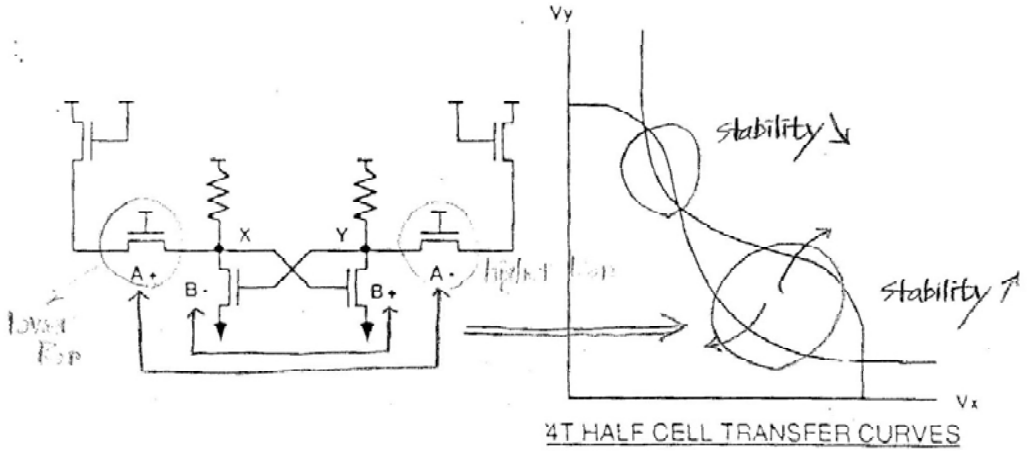


6T HALF CELL TRANSFER CURVES

compared to 4T cell

(better stability, physical size ↗ due to well separation)

MEMORY CELL ASYMETRY



4T HALF CELL TRANSFER CURVES

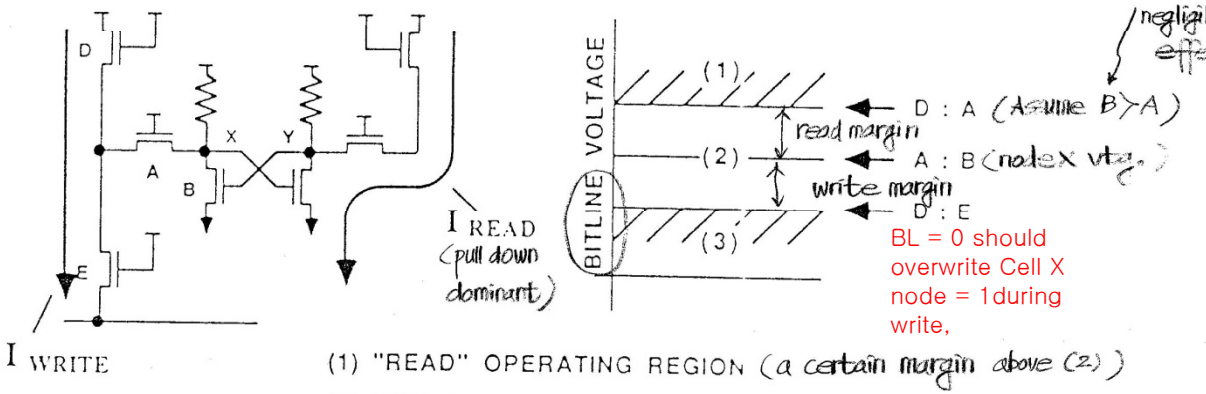
CAUSES:

- DESIGN MISMATCH - DIFFERENT LAYOUT/SIZE
- PROCESS MISMATCH - Vt, CDs, ETC
- ALIGNMENT SENSITIVITY → WIDTH, LENGTH

critical dimension

4T MEMORY CELL READ/WRITE OPERATION

Imagine voltage divider

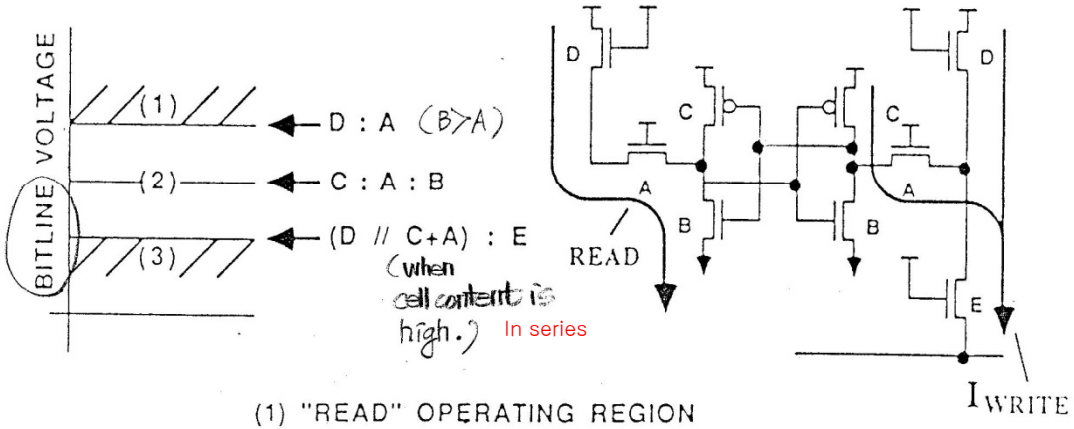


(1) "READ" OPERATING REGION (a certain margin above (2))

(2) MEM CELL "TRIP" VOLTAGE

(3) "WRITE" OPERATING REGION (a certain margin below (2))

6T MEMORY CELL READ/WRITE OPERATION

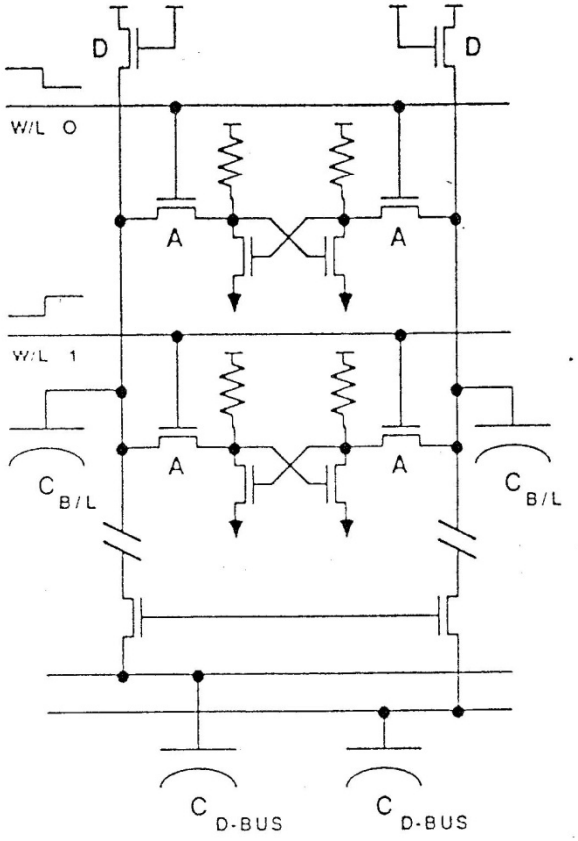


(1) "READ" OPERATING REGION

(2) MEM CELL "TRIP" VOLTAGE

(3) "WRITE" OPERATING REGION

MEMORY CELL SPEED VR. POWER



$Q = CV \longrightarrow I_{read} \cdot dt = C_{tot} \cdot dV$

$$dt = [\ C_{tot} / I_{read}\ ]\ dV$$

- dt: "SPEED"
- C_{tot}: CAP LOAD FIXED BY RAM DENSITY
- I_{read}: POWER FIXED BY PASS GATE SIZE - A
- dV: VOLTAGE SWING FIXED BY RATIO D : A

During read,
B effect is negligible
since it is large

DRAM - Dynamic Random-Access Memory

1988 IEDM Short Course on Microprocessor and Memories

Nicky C.-C. Lu

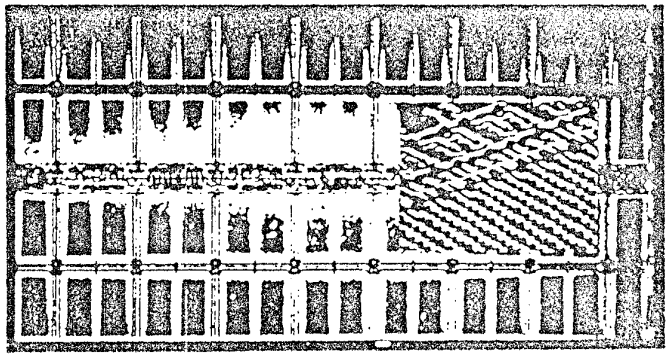
IBM Research Division
Thomas J. Watson Research Center, Yorktown Heights, NY 10598

1. DRAM And Its Development

1.1 Background And Definition
1.2 DRAMs in Systems: Examples
1.3 Product Environments And Trends

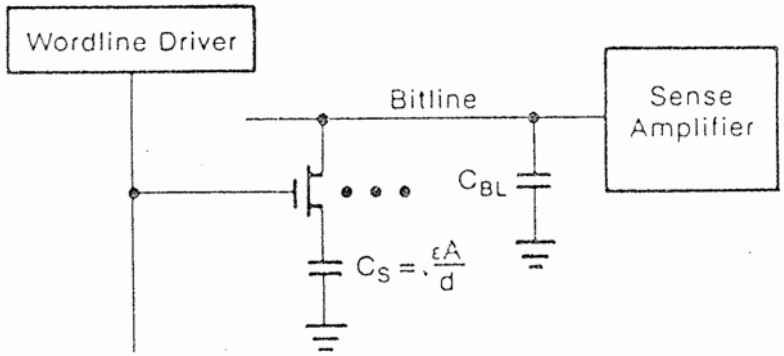
DRAM Chip

- Cell Arrays And Peripheral Circuits
- Array Utilization = (Cell Area × Total Bits)/(Chip Area)
- Key: Small Cell Area



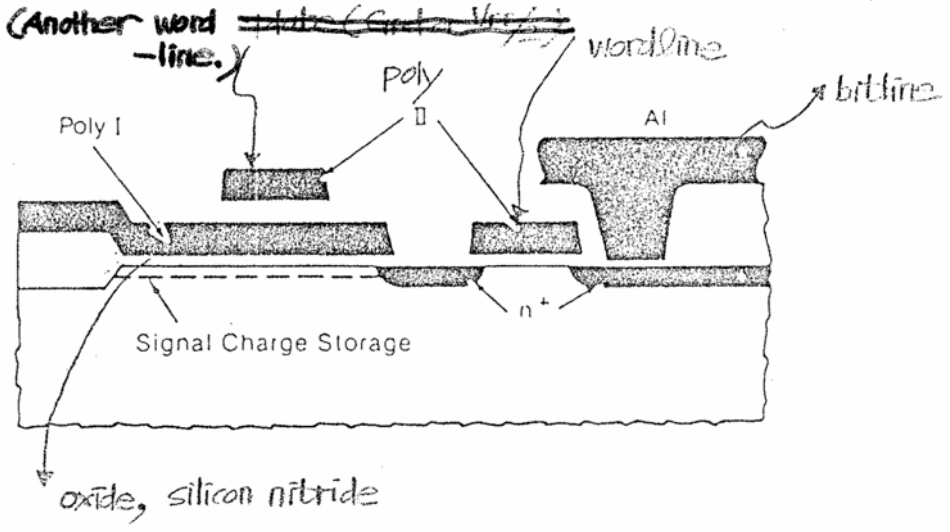
One-Transistor Cell

- An Access Transistor Plus A Storage Capacitor
  - — Selected By Wordline
  - — Signal Developed on Bitline



Planar Cell Structure

- Planar Transistor Plus Planar Capacitor in Silicon
- Uses Two Polysilicon Layers
- Storage-Node Leakage Requires Refreshing Data Periodically

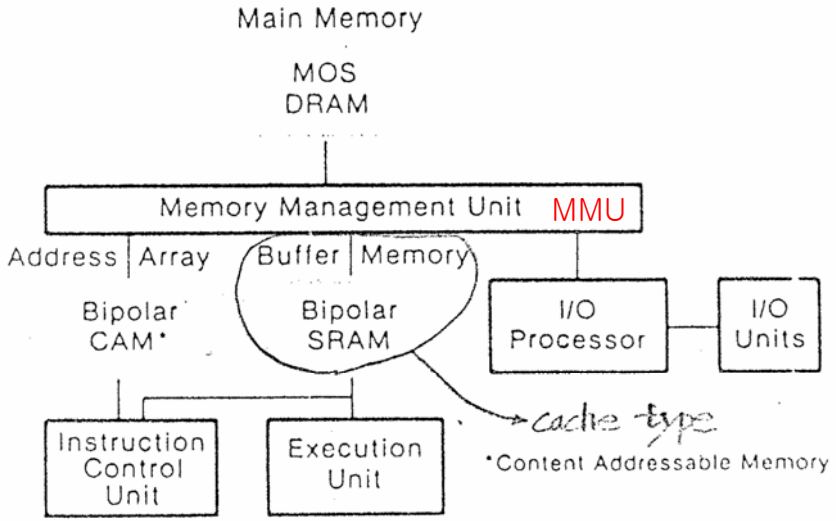


DRAM Definition

- Randomly Addressable Memory (Versus Serial Memory)
- Electrically Read and Write Data at Will in Any Sequence
- Needs Refresh Periodically
- Volatile (Unless By Battery Backup)

DRAM in Mainframe

- Today: ≃1GB (8,000 1Mb DRAM Chips)
- By 1995: ⩾64GB (Needs 8,000 64Mb DRAM Chips)



(Figure from Ref. B-6)

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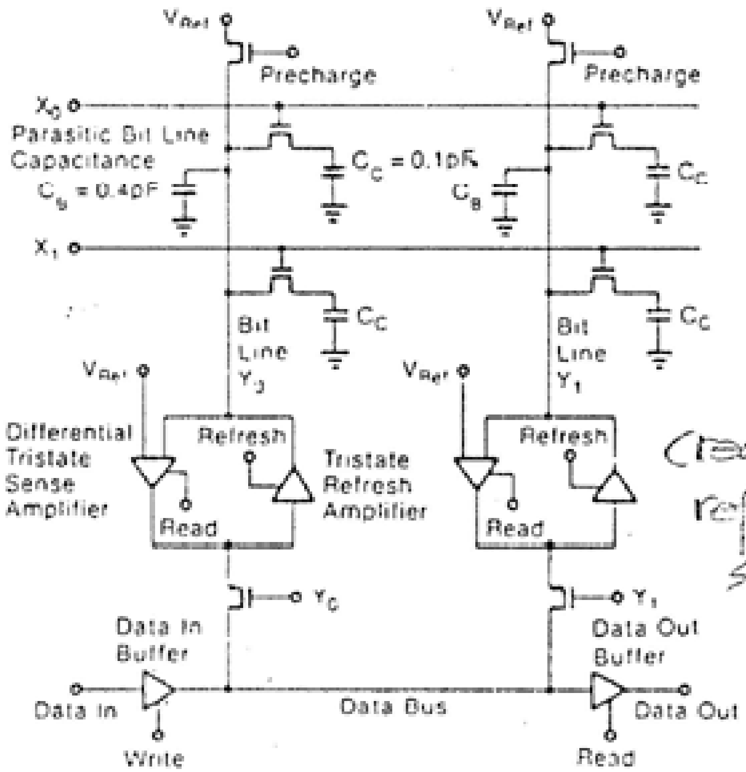
2. Chip/Circuit Design

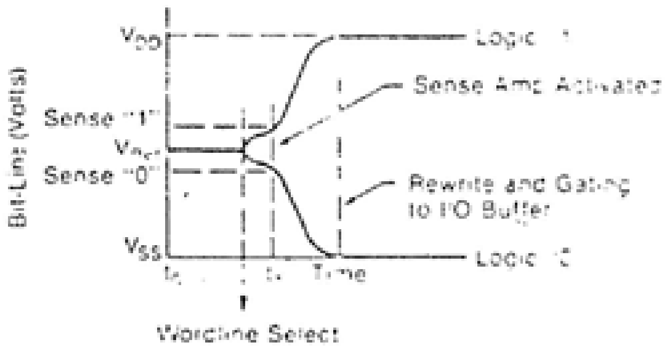
2.1 Basic DRAM Operations

2.2 Design Example: A 512Kb CMOS High Speed DRAM

2.3 Notes on NMOS and BiCMOS DRAMs

Basic Array Design





(read & refresh simultaneously.)

(After Ref.)

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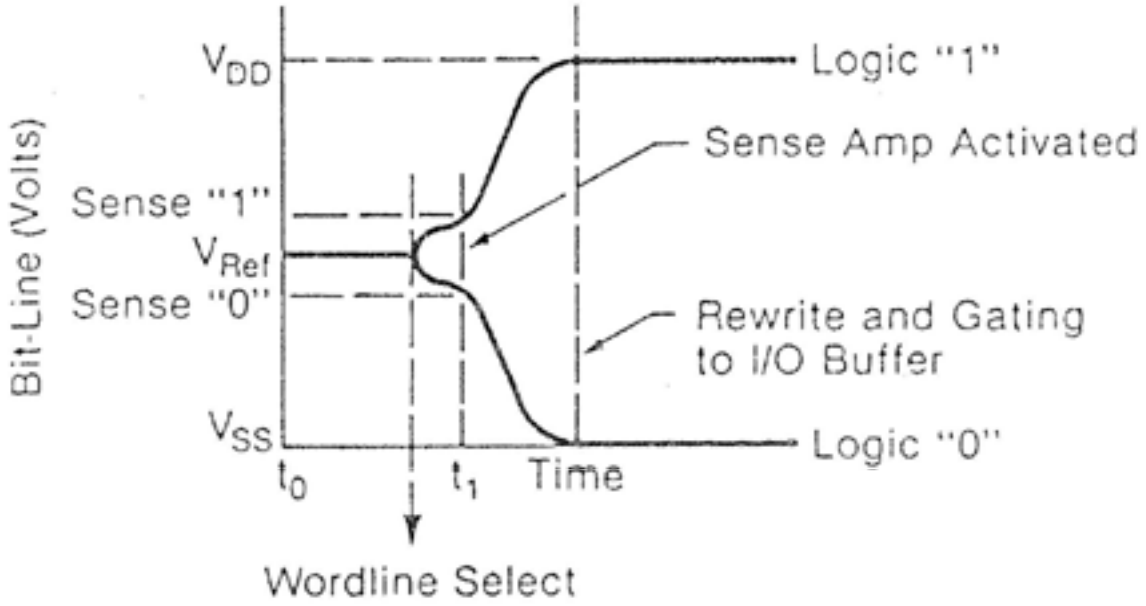
Signal Development



Charge Transfer Ratio Concept (During Read)

- $V_R(1) = \dfrac{C_s V(1) + C_B V_{ref}}{C_s + C_B}$ (charge sharing)

  C_s ; cell cap.
  C_B ; bit line cap.

- $\Delta V_{sen}(1) = V_R(1) - V_{ref} = \dfrac{C_s}{C_s + C_B}\,[V(1) - V_{ref}]$

  $\Delta V_{sen}(0) = V_{ref} - V_R(0) = \dfrac{C_s}{C_s + C_B}\,[V_{ref} - V(0)]$

- $V_{sen} = \dfrac{1}{2}\,[\Delta V_{sen}(1) + \Delta V_{sen}(0)] = \dfrac{1}{2}\,\dfrac{C_s}{C_s + C_B}\,\underbrace{[V(1) - V(0)]}_{V_s}$

  (average value)

- Transfer Ratio $T = \dfrac{C_s}{C_s + C_B}$ $\approx C_B$ (1 : 10)

- Storage Charge Capacity $Q_s = C_s V_s = 2(C_s + C_B)V_{sen}$

$V_{sen} = \dfrac{C_s V_s}{2(C_s + C_B)}$

$V_s \uparrow$ or $C_B \downarrow$

Cell Design Basics

- $V_{sen} + \Delta V = \frac{1}{2(C_S + C_B)} \cdot \frac{\varepsilon A V_S}{d}$

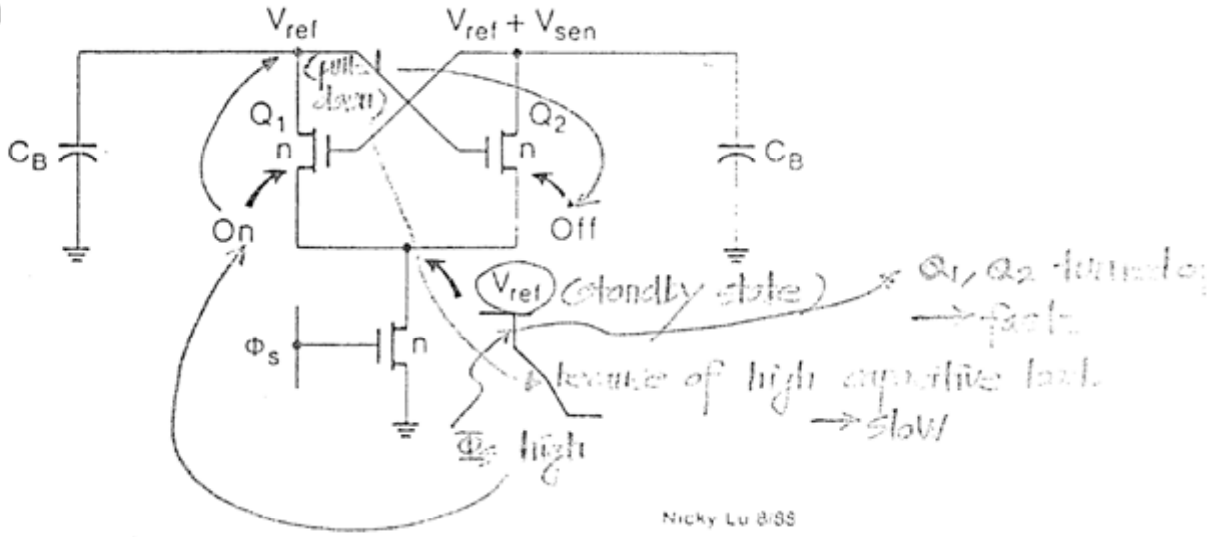
  C_S

  Where ΔV : Noise
  ε : Dielectric Constants
  A : Storage Area
  V_S : Storage Signal
  d : Dielectric Thickness

- V_S/d Limited By Maximum Dielectric Strength

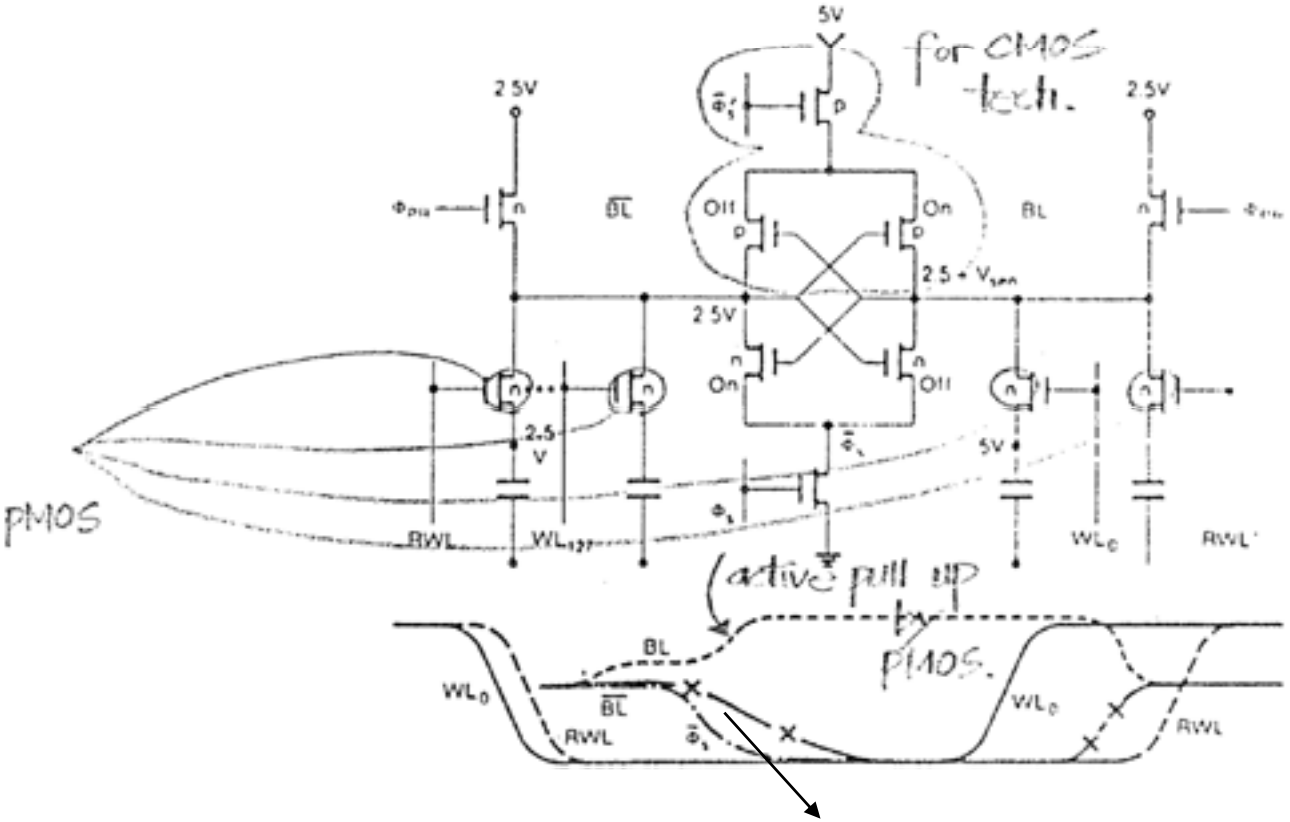
Cross-Coupled Sense Amplifier

- Differential Signal Established
- Latching
- Amplification



Sensing Circuits

- CMOS Cross-Coupled Latch



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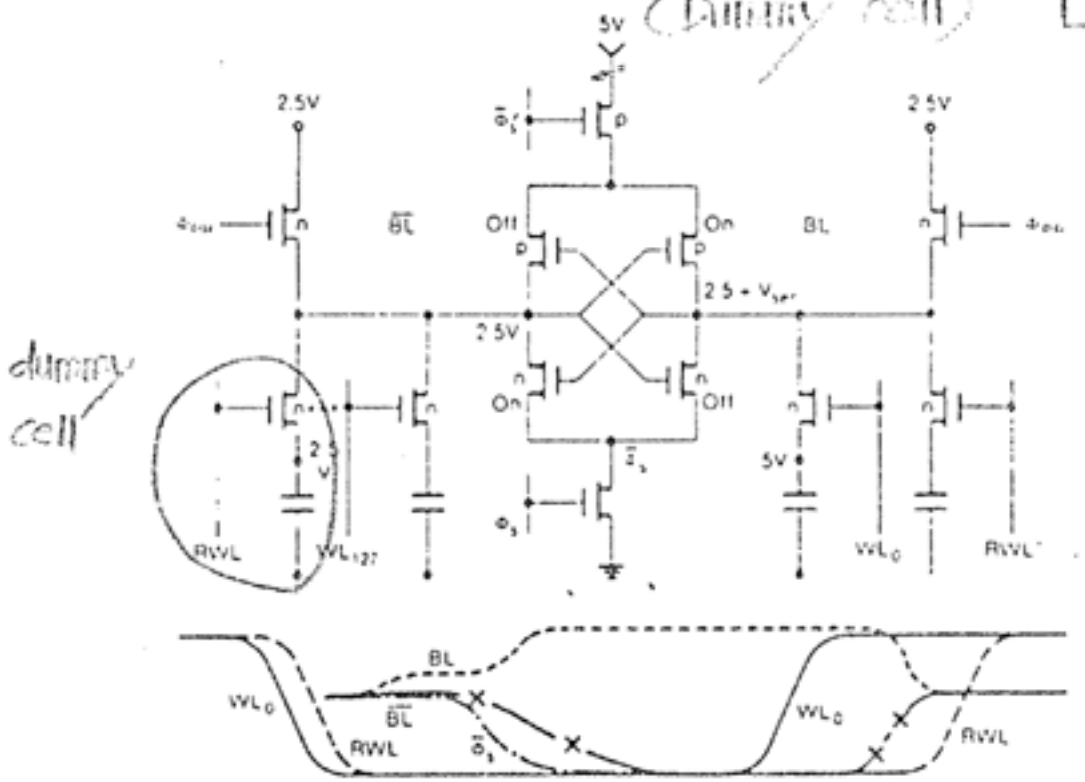
Phi pulled down then bit line change

Sensing Circuits

- Bitline Precharge
- Reference Cell Concept



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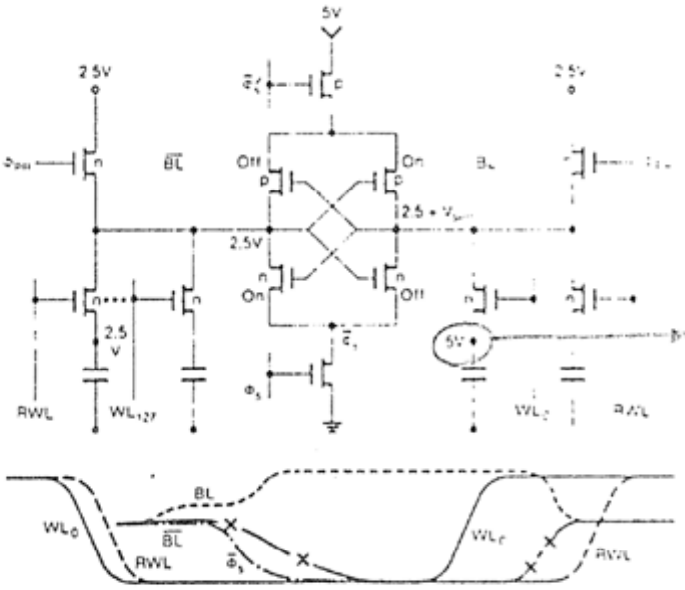
Sensing Circuits

- Self Restore
- Refresh



degraded while reading
(write back necessary)