

Introduction to CMOS VLSI Design

Lecture 16: Circuit Pitfalls

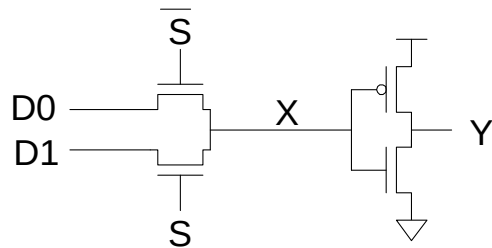
Outline

- ❑ Circuit Pitfalls
 - Detective puzzle
 - Given circuit and symptom, diagnose cause and recommend solution
 - All these pitfalls have caused failures in real chips
- ❑ Noise Budgets
- ❑ Reliability

Bad Circuit 1

❑ Circuit

- 2:1 multiplexer



❑ Principle:

❑ Solution:

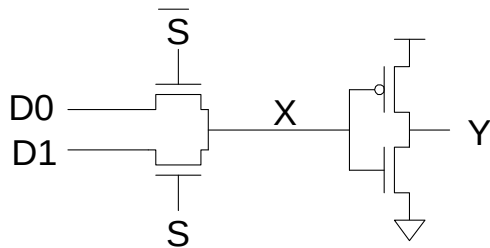
❑ Symptom

- Mux works when selected D is 0 but not 1.
- Or fails at low V_{DD} .
- Or fails in SFSF corner.

Bad Circuit 1

❑ Circuit

- 2:1 multiplexer



❑ Symptom

- Mux works when selected D is 0 but not 1.
- Or fails at low V_{DD} .
- Or fails in SFSF corner.
(NMOS-PMOS-voltage-temp corner)

❑ Principle: Threshold drop

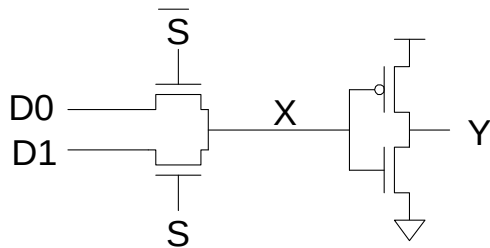
- X never rises above $V_{DD} - V_t$
- V_t is raised by the body effect
- The threshold drop is most serious as V_t becomes a greater fraction of V_{DD} .

❑ Solution:

Bad Circuit 1

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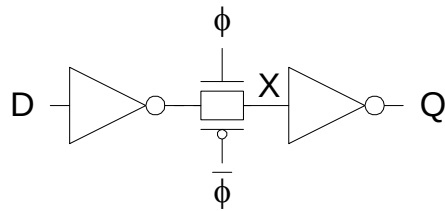
- X never rises above $V_{DD} - V_t$
- V_t is raised by the body effect
- The threshold drop is most serious as V_t becomes a greater fraction of V_{DD} .

❑ Solution: Use transmission gates, not pass transistors

Bad Circuit 2

❑ Circuit

- Latch



❑ Symptom

- Load a 0 into Q
- Set $\phi = 0$
- Eventually Q spontaneously flips to 1

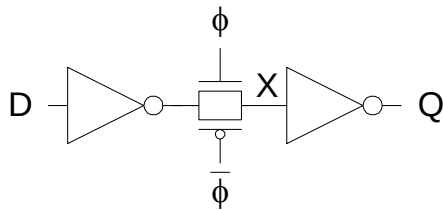
❑ Principle:

❑ Solution:

Bad Circuit 2

❑ Circuit

- Latch



❑ Symptom

- Load a 0 into Q
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❑ Principle: Leakage

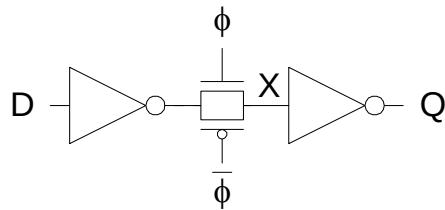
- X is a dynamic node holding value as charge on the node
- Eventually subthreshold leakage may disturb charge

❑ Solution:

Bad Circuit 2

❑ Circuit

- Latch



❑ Symptom

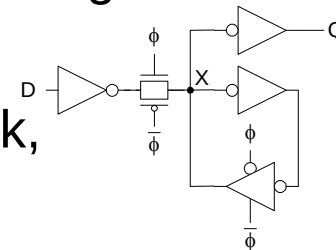
- Load a 0 into Q
- Set $\phi = 0$
- Eventually Q spontaneously flips to 1

❑ Principle: Leakage

- X is a dynamic node holding value as charge on the node
- Eventually subthreshold leakage may disturb charge

❑ Solution: Staticize node with feedback

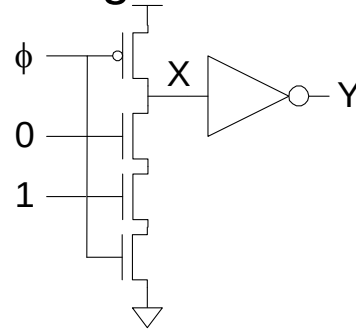
- Or periodically refresh node (requires fast clock, not practical processes with big leakage)



Bad Circuit 3

❑ Circuit

- Domino AND gate



❑ Symptom

- Precharge gate ($Y=0$)
- Then evaluate
- Eventually Y spontaneously flips to 1

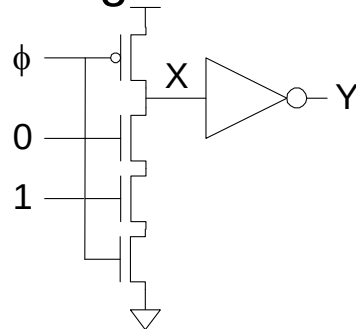
❑ Principle:

❑ Solution:

Bad Circuit 3

❑ Circuit

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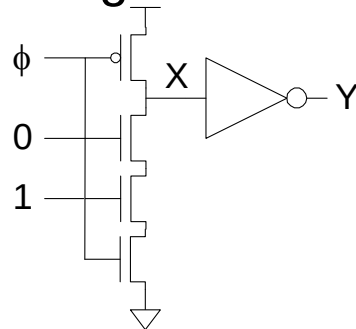
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Bad Circuit 3

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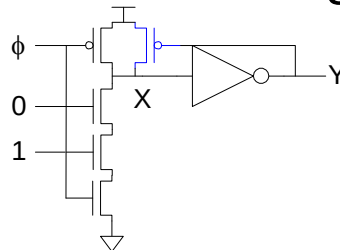
❑ Symptom

- Precharge gate ($Y=0$)
- Then evaluate
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- X is a dynamic node holding value as charge on the node
- Eventually subthreshold leakage may disturb charge

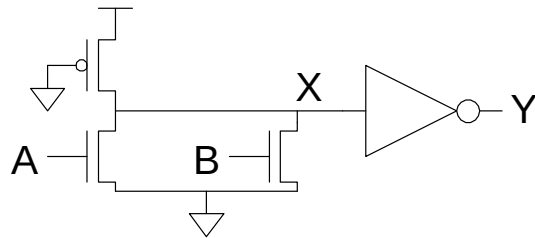
❑ Solution: Keeper



Bad Circuit 4

❑ Circuit

- Pseudo-nMOS OR



❑ Symptom

- When only one input is true, $Y = 0$.
- Perhaps only happens in SF (NMOS-PMOS) corner.

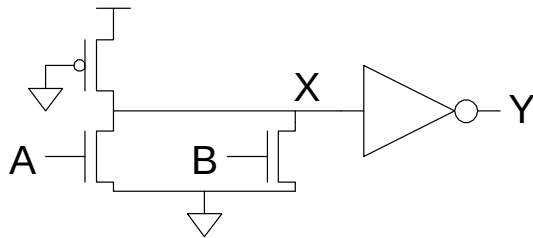
❑ Principle:

❑ Solution:

Bad Circuit 4

❑ Circuit

- Pseudo-nMOS OR



❑ Symptom

- When only one input is true, $Y = 0$.
- Perhaps only happens in SF corner.

❑ Principle: Ratio Failure

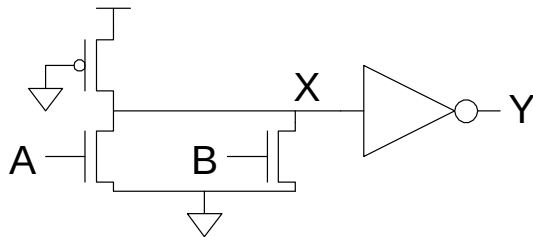
- nMOS and pMOS fight each other.
- If the pMOS is too strong, nMOS cannot pull X low enough.

❑ Solution:

Bad Circuit 4

❑ Circuit

- Pseudo-nMOS OR



❑ Symptom

- When only one input is true, $Y = 0$.
- Perhaps only happens in SF corner.

❑ Principle: Ratio Failure

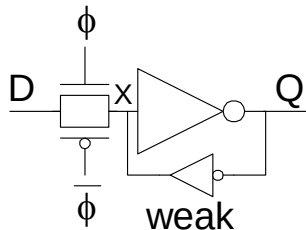
- nMOS and pMOS fight each other.
- If the pMOS is too strong, nMOS cannot pull X low enough.

❑ Solution: Check that ratio is satisfied in all corners

Bad Circuit 5

❑ Circuit

- Latch



❑ Principle:

❑ Solutions:

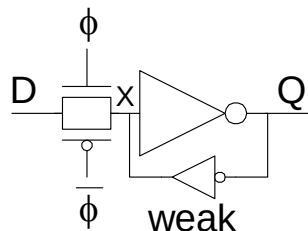
❑ Symptom

- Q stuck at 1.
- May only happen for certain latches where input is driven by a small gate located far away.

Bad Circuit 5

❑ Circuit

- Latch

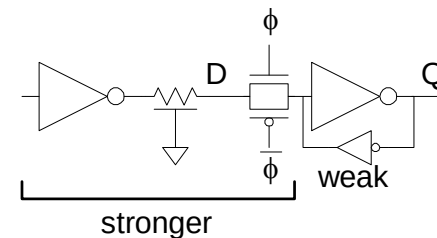


❑ Symptom

- Q stuck at 1.
- May only happen for certain latches where input is driven by a small gate located far away.

❑ Principle: Ratio Failure (again)

- Series resistance of D driver, wire resistance, and t_{gate} must be much less than weak feedback inverter.

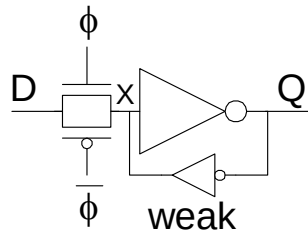


❑ Solutions:

Bad Circuit 5

❑ Circuit

- Latch

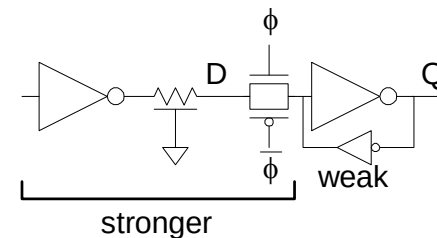


❑ Symptom

- Q stuck at 1.
- May only happen for certain latches where input is driven by a small gate located far away.

❑ Principle: Ratio Failure (again)

- Series resistance of D driver, wire resistance, and tgate must be much less than weak feedback inverter.



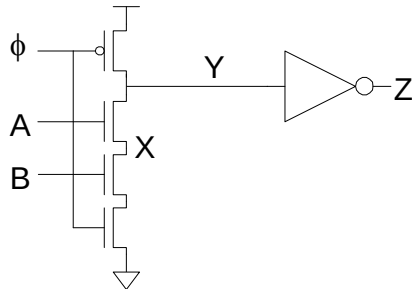
❑ Solutions: Check relative strengths

- Avoid unbuffered diffusion inputs where driver is unknown

Bad Circuit 6

Circuit

- Domino AND gate



 Principle:

 Solutions:

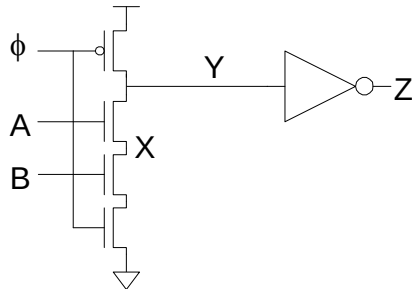
☐ Symptom

- Precharge gate while $A = B = 0$, so $Z = 0$
- Set $\phi = 1$
- A rises
- Z is observed to sometimes rise

Bad Circuit 6

❑ Circuit

- Domino AND gate



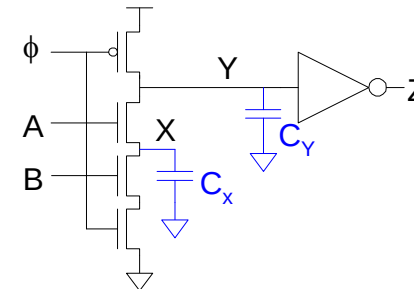
❑ Principle: Charge Sharing

- If X was low, it shares charge with Y

❑ Solutions:

❑ Symptom

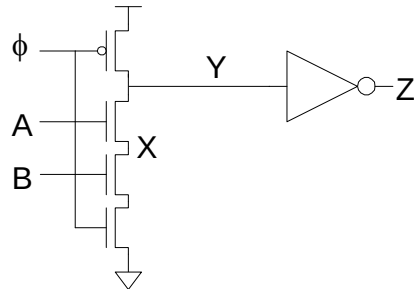
- Precharge gate while $A = B = 0$, so $Z = 0$
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- A rises
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Bad Circuit 6

❑ Circuit

- Domino AND gate



❑ Principle: Charge Sharing

- If X was low, it shares charge with Y

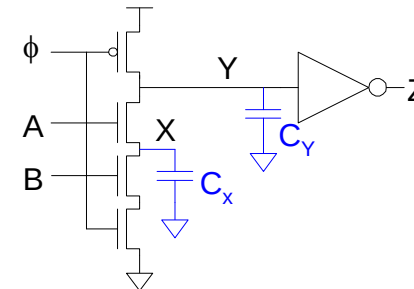
❑ Solutions: Limit charge sharing

$$V_x = V_Y = \frac{C_Y}{C_x + C_Y} V_{DD}$$

- Safe if $C_Y \gg C_X$
- Or precharge node X too

❑ Symptom

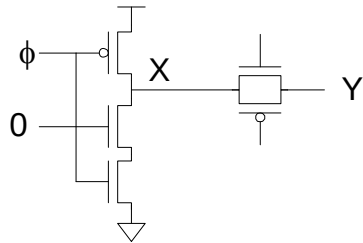
- Precharge gate while $A = B = 0$, so $Z = 0$
- Set $\phi = 1$
- A rises
- Z is observed to sometimes rise



Bad Circuit 7

❑ Circuit

- Dynamic gate + latch



❑ Principle:

❑ Solution:

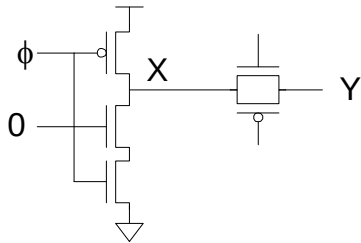
❑ Symptom

- Precharge gate while transmission gate latch is opaque
- Evaluate
- When latch becomes transparent, X falls

Bad Circuit 7

❑ Circuit

- Dynamic gate + latch



❑ Principle: Charge Sharing

- If Y was low, it shares charge with X

❑ Solution:

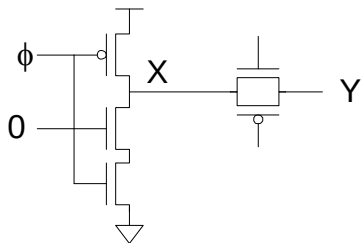
❑ Symptom

- Precharge gate while transmission gate latch is opaque
- Evaluate
- When latch becomes transparent, X falls

Bad Circuit 7

❑ Circuit

- Dynamic gate + latch



❑ Principle: Charge Sharing

- If Y was low, it shares charge with X (X doesn't stay high as precharged)

❑ Solution: Buffer dynamic nodes before driving transmission gate

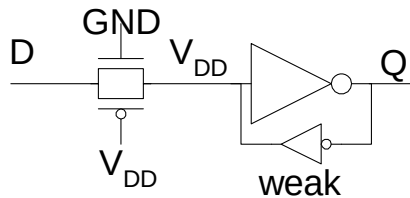
❑ Symptom

- Precharge gate while transmission gate latch is opaque
- Evaluate
- When latch becomes transparent, X falls

Bad Circuit 8

❑ Circuit

- Latch



❑ Symptom

- Q changes while latch is opaque
- Especially if D comes from a far-away driver

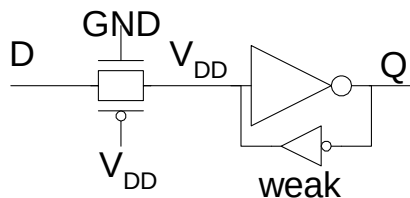
❑ Principle:

❑ Solution:

Bad Circuit 8

❑ Circuit

- Latch



❑ Symptom

- Q changes while latch is opaque
- Especially if D comes from a far-away driver

❑ Principle: Diffusion Input Noise Sensitivity

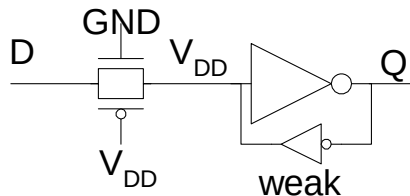
- If $D < -V_t$, transmission gate turns on
- Most likely because of power supply noise or coupling on D

❑ Solution:

Bad Circuit 8

❑ Circuit

- Latch



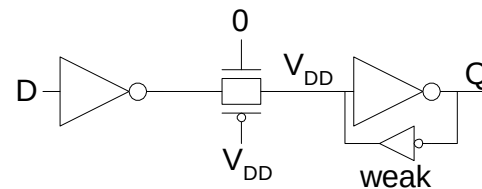
❑ Symptom

- Q changes while latch is opaque
- Especially if D comes from a far-away driver

❑ Principle: Diffusion Input Noise Sensitivity

- If $D < -V_t$, transmission gate turns on
- Most likely because of power supply noise or coupling on D

❑ Solution: Buffer D locally



Bad Circuit 9

- ❑ Circuit

- Anything

- ❑ Symptom

- Some gates are slower than expected

- ❑ Principle:

Bad Circuit 9

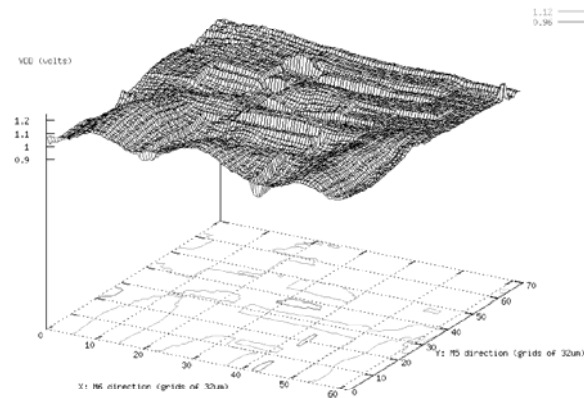
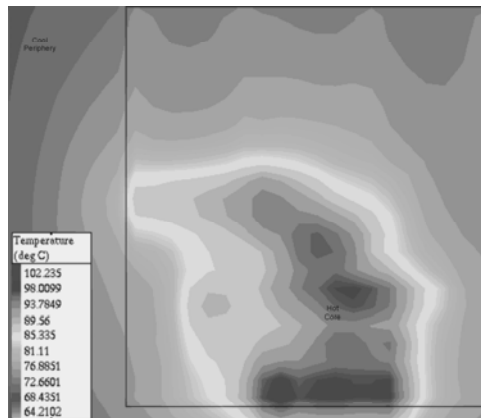
❑ Circuit

- Anything

❑ Symptom

- Some gates are slower than expected

❑ Principle: Hot Spots and Power Supply Noise



Noise

❑ Sources

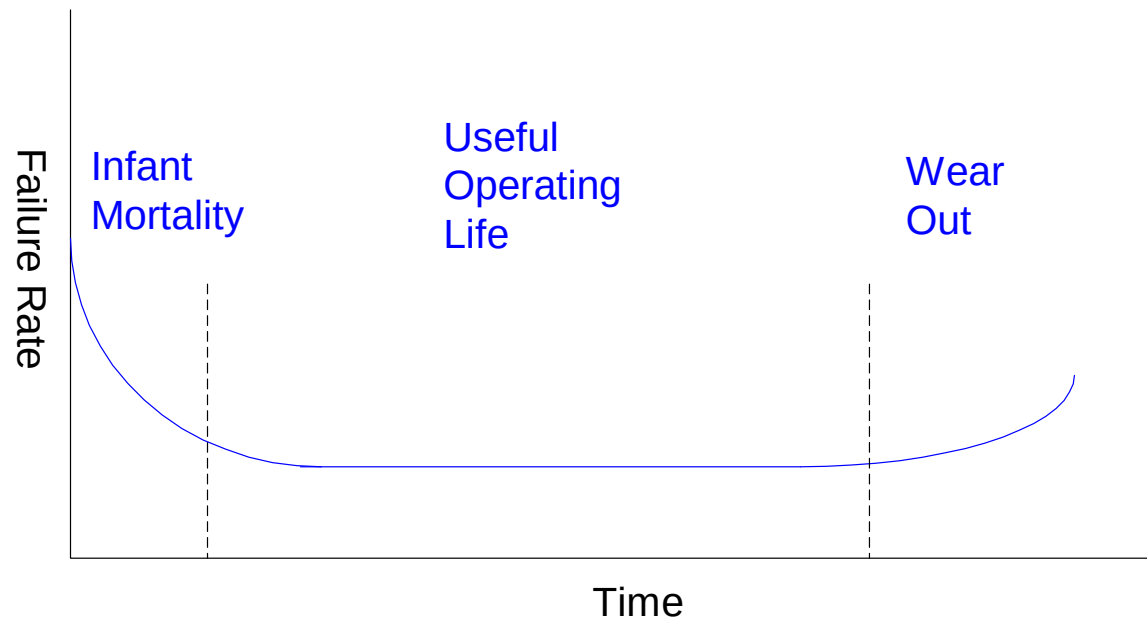
- Power supply noise / ground bounce
- Capacitive coupling
- Charge sharing
- Leakage
- Noise feedthrough

❑ Consequences

- Increased delay (for noise to settle out)
- Or incorrect computations

Reliability

- ❑ Hard Errors
- ❑ Soft Errors



Electromigration

- ❑ “Electron wind” causes movement of metal atoms along wires
- ❑ Excessive electromigration leads to open circuits
- ❑ Most significant for unidirectional (DC) current
 - Depends on current density J_{dc} (current / area)
 - Exponential dependence on temperature
 - Black’s Equation: $MTTF \propto \frac{e^{\frac{E_a}{kT}}}{J_{dc}^n}$
MTTF: Mean Time To Failures
 - Typical limits: $J_{dc} < 1 - 2 \text{ mA} / \mu\text{m}^2$
- ❑ See videos

Self-Heating

- ❑ Current through wire resistance generates heat
 - Oxide surrounding wires is a thermal insulator
 - Heat tends to build up in wires
 - Hotter wires are more resistive, slower
- ❑ Self-heating limits AC current densities for reliability

$$I_{rms} = \sqrt{\frac{\int_0^T I(t)^2 dt}{T}}$$

- Typical limits: $J_{rms} < 15 \text{ mA} / \mu\text{m}^2$

Hot Carriers

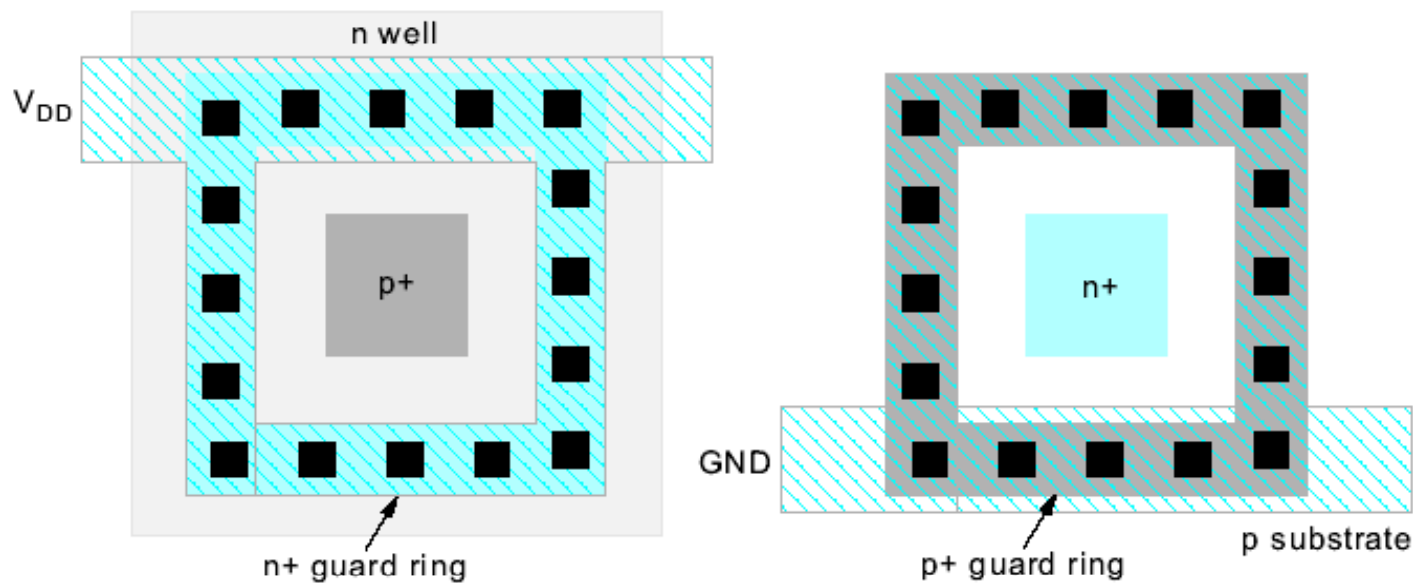
- ❑ Electric fields across channel impart high energies to some carriers
 - These “hot” carriers may be blasted into the gate oxide where they become trapped
 - Accumulation of charge in oxide causes shift in V_t over time
 - Eventually V_t shifts too far for devices to operate correctly
- ❑ Choose V_{DD} to achieve reasonable product lifetime
 - Worst problems for inverters and NORs with slow input risetime and long propagation delays

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Guard Rings

- ❑ Latchup risk greatest when diffusion-to-substrate diodes could become forward-biased
- ❑ Surround sensitive region with guard ring to collect injected charge



Overvoltage

- ❑ High voltages can damage transistors
 - Electrostatic discharge
 - Oxide arcing → Metal line damage
 - Punchthrough
 - Time-dependent dielectric breakdown (TDDB)
 - Accumulated wear from tunneling currents
- ❑ Requires low V_{DD} for thin oxides and short channels
- ❑ Use ESD protection structures where chip meets real world

Summary

- ❑ Static CMOS gates are very robust
 - Will settle to correct value if you wait long enough
- ❑ Other circuits suffer from a variety of pitfalls
 - Tradeoff between performance & robustness
- ❑ Very important to check circuits for pitfalls
 - For large chips, you need an automatic checker.
 - Design rules aren't worth the paper they are printed on unless you back them up with a tool.

Soft Errors

- ❑ In 1970's, DRAMs were observed to occasionally flip bits for no apparent reason
 - Ultimately linked to alpha particles and cosmic rays
- ❑ Collisions with particles create electron-hole pairs in substrate
 - These carriers are collected on dynamic nodes, disturbing the voltage
- ❑ Minimize soft errors by having plenty of charge on dynamic nodes
- ❑ Tolerate errors through ECC, redundancy