Introduction to CMOS VLSI Design

Lecture 18: Design for Low Power

Outline

- Power and Energy
- Dynamic Power
- Static Power
- Low Power Design

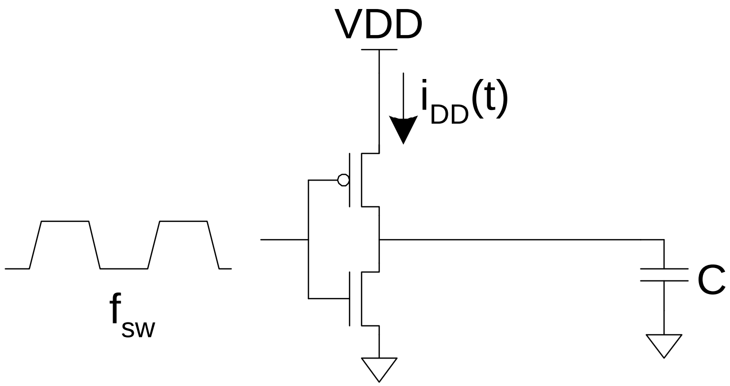
Power and Energy

- Power is drawn from a voltage source attached to the V_{DD} pin(s) of a chip.
- Instantaneous Power: $P(t) = i_{DD}(t)V_{DD}$
- Energy: $E = \int_0^T P(t)dt = \int_0^T i_{DD}(t)V_{DD}dt$
- Average Power: $P_{\text{avg}} = \frac{E}{T} = \frac{1}{T}\int_0^T i_{DD}(t)V_{DD}dt$

Dynamic Power

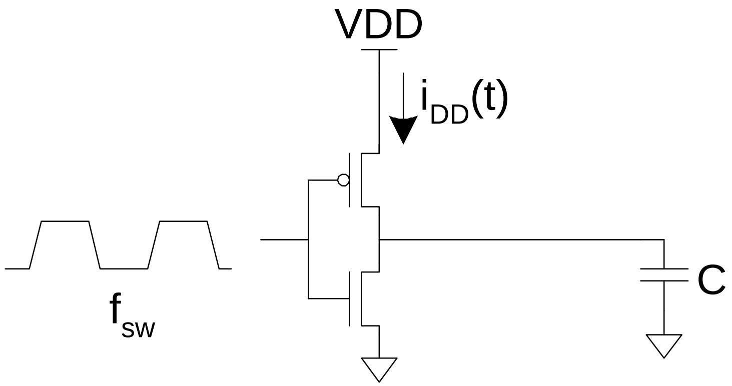
- Dynamic power is required to charge and discharge load capacitances when transistors switch.

- One cycle involves a rising and falling output.
- On rising output, charge $Q = CV_{DD}$ is required
- On falling output, charge is dumped to GND
- This repeats Tf_{sw} times over an interval of T



Dynamic Power Cont.

$$P_{\text{dynamic}} =$$



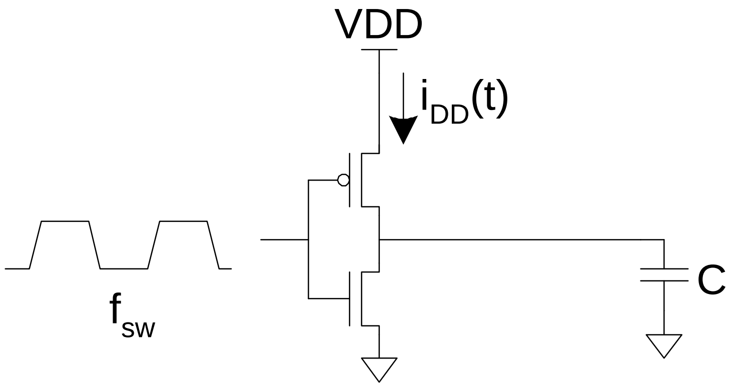
Dynamic Power Cont.

$$P_{\text{dynamic}} = \frac{1}{T}\int_0^T i_{DD}(t)V_{DD}\,dt$$

$$= \frac{V_{DD}}{T}\int_0^T i_{DD}(t)\,dt$$

$$= \frac{V_{DD}}{T}\left[Tf_{\text{sw}}CV_{DD}\right]$$

$$\boxed{= CV_{DD}^{\ 2} f_{\text{sw}}}$$



Activity Factor

- Suppose the system clock frequency = f
- Let $f_{sw} = \alpha f$, where α = activity factor
  - If the signal is a clock, $\alpha = 1$
  - If the signal switches once per cycle, $\alpha = ½$

    (for 1/2 period, signal = high, consuming power)
  - Dynamic gates:
    - Switch either 0 or 2 times per cycle, $\alpha = ½$
  - Static gates:
    - Depends on design, but typically $\alpha = 0.1$
- Dynamic power: $P_{\text{dynamic}} = \alpha C V_{DD}^2 f$

Short Circuit Current

- When transistors switch, both nMOS and pMOS networks may be momentarily ON at once
- Leads to a blip of “short circuit” current.
- < 10% of dynamic power if rise/fall times are comparable for input and output (slower → more power)

Example

- 200 M transistor chip
  - 20M logic transistors
    - Average width: 12 λ
  - 180M memory transistors
    - Average width: 4 λ
  - 1.2 V 100 nm process
  - C_g = 2 fF/μm

Dynamic Example

- Static CMOS logic gates: activity factor = 0.1
- Memory arrays: activity factor = 0.05 (many banks!)

- Estimate dynamic power consumption per MHz. Neglect wire capacitance and short-circuit current.

Dynamic Example

- Static CMOS logic gates: activity factor = 0.1
- Memory arrays: activity factor = 0.05 (many banks!)

- Estimate dynamic power consumption per MHz. Neglect wire capacitance.

$$C_{\text{logic}} = \left(20\times10^{6}\right)\left(12\lambda\right)\left(0.05\mu m/\lambda\right)\left(2\,fF/\mu m\right) = 24nF$$

$$C_{\text{mem}} = \left(180\times10^{6}\right)\left(4\lambda\right)\left(0.05\mu m/\lambda\right)\left(2\,fF/\mu m\right) = 72nF$$

$$P_{\text{dynamic}} = \left[0.1C_{\text{logic}} + 0.05C_{\text{mem}}\right]\overset{\text{VDD}}{\left(1.2\right)}^{2} f = 8.6\text{ mW/MHz}$$

Static Power

- Static power is consumed even when chip is quiescent.
  - Ratioed circuits burn power in fight between ON transistors
  - Leakage draws power from nominally OFF devices

$$I_{ds} = I_{ds0} e^{\frac{V_{gs} - V_t}{n v_T}} \left[1 - e^{\frac{-V_{ds}}{v_T}} \right]$$

$$V_t = V_{t0} - \eta V_{ds} + \gamma \left(\sqrt{\phi_s + V_{sb}} - \sqrt{\phi_s} \right)$$

Ratio Example

- The chip contains a 32 word x 48 bit ROM
  - Uses pseudo-nMOS decoder and bitline pullups
  - On average, one wordline and 24 bitlines (bit and bit/ so 24 X 2=48) are high
- Find static power drawn by the ROM
  - $\beta = 75\ \mu A/V^2$
  - $V_{tp} = -0.4V$

Ratio Example

- The chip contains a 32 word x 48 bit ROM
  - Uses pseudo-nMOS decoder and bitline pullups
  - On average, <u>one wordline and 24 bitlines are high</u>
- Find static power drawn by the ROM
  - $\beta = 75\ \mu A/V^2$
  - $V_{tp} = -0.4V$
- Solution:

24 bit lines = ½ of 48 bits
(one of bit or bit/ is high)
One word line activates
the 24 bit lines

Only one of 32 word lines is high
and the rest are low consuming
pull up power.due to pseudo nMOS

$$I_{\text{pull-up}} = \beta \frac{\left(V_{DD} - \left|V_{tp}\right|\right)^2}{2} = 24\mu\text{A}$$

$$P_{\text{pull-up}} = V_{DD} I_{\text{pull-up}} = 29\mu\text{W}$$

$$P_{\text{static}} = (31 + 24) P_{\text{pull-up}} = 1.6\ \text{mW}$$

Leakage Example

- The process has two threshold voltages and two oxide thicknesses.
- Subthreshold leakage:
  - 20 nA/μm for low V_t
  - 0.02 nA/μm for high V_t
- Gate leakage (gate oxide perimeter and so on):
  - 3 nA/μm for thin oxide
  - 0.002 nA/μm for thick oxide
- <u>Memories use low-leakage transistors everywhere</u>
- Gates use low-leakage transistors on 80% of logic

Leakage Example Cont.

- Estimate static power:

Leakage Example Cont.

- Estimate static power: 80% of logic uses low leakage
  - High leakage: $\left(20\times10^{6}\right)\boxed{\left(0.2\right)}\left(12\lambda\right)\left(0.05\mu m/\lambda\right)=2.4\times10^{6}\ \mu m$
  - Low leakage: $\left(20\times10^{6}\right)\boxed{\left(0.8\right)}\left(12\lambda\right)\left(0.05\mu m/\lambda\right)+$

$$\left(180\times10^{6}\right)\left(4\lambda\right)\left(0.05\mu m/\lambda\right)=45.6\times10^{6}\ \mu m$$

$$I_{static}=\left(2.4\times10^{6}\ \mu m\right)\left[\left(20nA/\mu m\right)/2+\left(3nA/\mu m\right)\right]+$$

Subthreshold and leakage

$$\left(45.6\times10^{6}\ \mu m\right)\left[\left(0.02nA/\mu m\right)/2+\left(0.002nA/\mu m\right)\right]$$

$$=32mA$$

$$P_{static}=I_{static}V_{DD}=38mW$$

Leakage Example Cont.

- Estimate static power:
  - High leakage: $\left(20\times10^{6}\right)\left(0.2\right)\left(12\lambda\right)\left(0.05\mu m/\lambda\right)=2.4\times10^{6}\,\mu m$
  - Low leakage: $\left(20\times10^{6}\right)\left(0.8\right)\left(12\lambda\right)\left(0.05\mu m/\lambda\right)+$
    $\left(180\times10^{6}\right)\left(4\lambda\right)\left(0.05\mu m/\lambda\right)=45.6\times10^{6}\,\mu m$

$$
\begin{aligned}
I_{static} &= \left(2.4\times10^{6}\,\mu m\right)\left[\left(20nA/\mu m\right)/2+\left(3nA/\mu m\right)\right]+ \\
&\quad \left(45.6\times10^{6}\,\mu m\right)\left[\left(0.02nA/\mu m\right)/2+\left(0.002nA/\mu m\right)\right] \\
&= 32mA
\end{aligned}
$$

$$P_{static} = I_{static}V_{DD} = 38mW$$

- If no low leakage devices, P_{static} = 749 mW (!)

Low Power Design

- ❑ Reduce dynamic power
  - α:
  - C:
  - V_{DD}:
  - f:
- ❑ Reduce static power

Low Power Design

- Reduce dynamic power
  - α: clock gating, sleep mode
  - C:
  - V_{DD}:
  - f:
- Reduce static power

Low Power Design

- Reduce dynamic power
  - α: clock gating, sleep mode
  - C: small transistors (esp. on clock), short wires
  - V_{DD}:
  - f:
- Reduce static power

Low Power Design

- Reduce dynamic power
  - α: clock gating, sleep mode
  - C: small transistors (esp. on clock), short wires
  - V_{DD}: lowest suitable voltage
  - f:
- Reduce static power

Low Power Design

- Reduce dynamic power
  - α: clock gating, sleep mode
  - C: small transistors (esp. on clock), short wires
  - V_{DD}: lowest suitable voltage
  - f: lowest suitable frequency
- Reduce static power

Low Power Design

- Reduce dynamic power
  - α: clock gating, sleep mode
  - C: small transistors (esp. on clock), short wires
  - V_{DD}: lowest suitable voltage
  - f: lowest suitable frequency
- Reduce static power
  - Selectively use ratioed circuits
  - Selectively use low V_t devices
  - Leakage reduction:
    stacked devices, body bias, low temperature